Radius FPD/SE Clone: Progress Synopsis

Reverse engineering the 1986 first-generation 64/68 Hz Full Page Display card for the Mac SE. Covers 261002 to 261102.

Where things stand

The test bench is up, the card is well mapped, and the plan has changed. If the buzz-out finishes cleanly, I may skip the drill map and go straight to a new PCB built from the netlist. Most of the work this month was tracing, plus a long design session on how the finished card should look.

Done on the bench and the board

- **Test stand:** the SE logic board is on a plexi carrier on my open SE/30 test stand, with a BlueSCSI on a slide-in carrier on the PSU. SE + MagicBus + FPD boots to the flashing question-mark floppy. A right-angle DIN 96 wire-wrap connector seats in the PDS slot.
- **Board construction:** it looks to be a 4-layer board with a solid inner plane. Much of the buried inner-layer net is now mapped, and it serves the empty U25/U26 "BigROM" footprints.
- **Artwork:** pinouts for 20 ICs are on the board registration, with confidence-coded trace layers and draft block and functional diagrams from 261029.
- **Data bus map, drawn from the artwork:** U16 = D0-D3, U15 = D4-D7, U12 = D8-D11, U11 = D12-D15. ROMs: Ux = D0-D7, U19 = D8-D15.
- **Syncs, buzz-confirmed 261031:** J1 pin 9 V-sync traces through R1 to U8 pin 17, and J1 pin 7 H-sync through R2 to U8 pin 18. Syncs come from U8, not U22 as first drawn.
- **Clocks:** Y1 51.270 MHz (64 Hz) and Y2 55.000 MHz (68 Hz), selected by JP1 as the pixel clock. Inferred timing is 800 x 1000 totals, or 68.75 kHz / 68.75 Hz at 55 MHz. Not yet measured.
- **MagicBus pinout:** all 60 lines check against Apple's Table 13-1: 50 signals plus 10 power and ground. The FPD never sees FC0-2, /VPA, /VMA, /BR, /BG, /BGACK, /PMCYC, /HALT, /IPL0, /IPL2 or /BERR.

Design conclusions so far

Topic	Current thinking	Basis
Build path	Bench card first: TTL and J1 kept, no FPGA, borrowed GALs and ROMs. Then split into North 40 (FPGA) and South 40 (VRAM, U9, ROM).	Avoids desoldering for a scan; proves the netlist
Bus level shifting	SE bus is 63 signals, not 80+. FPD needs 31 input lines plus /DTACK, /EXT.DTK and /IPL1: 5 chips and a single gate (3 and a gate with 16-bit parts).	Apple Table 13-1; part counts are my estimate
Card envelope	213.25 x 120.42 mm, 16 mm traces-only band, 15.58 to 4.61 mm clearance above the card, 16.8 mm below. Wire-wrap is bench-only.	Apple Figures 14-1 to 14-3
Power	Slot limit is 1.5 A at +5 V and about 7 W to 7.5 W. External USB-C can carry the FPGA rail, but the heat limit still applies. Keep the rails separate.	Apple Table 13-3 and heat guidelines
Rear panel	Connector board in the style of Bolle's 10BT breakout: DVI-D, USB-C power, and an optional unsupported antenna hole.	Apple Foldout 4; fit still to confirm
Boot behavior	Hold /RESET until the FPGA loads, if needed. A rear switch on the sense line chooses portrait display or internal screen.	Proposed; needs testing
VRAM, near term	Toshiba TC524256Z ZIP on a DIP carrier, A8 tied low. A pin map is done. Must check that WE stays high during transfers.	NEC and Toshiba datasheets; not tested

Topic	Current thinking	Basis
VRAM, GitHub build	One 5 V 64K x 16 SRAM (CY7C1021D), either behind a CPLD VRAM emulator with stock GALs, or with new logic at the FPGA stage.	Concept only

Still open

- Finish the buzz-out, including the buried net, then capture the netlist.
- GAL readout. Their functions are inferred from what they drive and read, so nothing about them is confirmed.
- WE during a VRAM transfer, and SC pulses per transfer, on a working card. A USB logic analyzer should cover both, plus sync frequencies.
- Get a System 6.0.8 boot going so both FPD cards can be tested with video.
- Finish the MagicBus-clone adapter PCB in KiCad, for its 0.075 in staggered JAE footprint.

Items marked inferred or proposed are not yet confirmed on hardware. Signal timing and Extron settings are still to be measured. Connector and bus figures are from Designing Cards and Drivers for the Macintosh II and Macintosh SE (Apple, 1987), and from the NEC and Toshiba data sheets.