PigPenMini: 68030 Performer + P2 memory port prototype for the Mac SE PDS

BEST-GUESS DRAFT 261126 for review. jt TrashBO / FPD clone / Pig Pen

Performer core (U1, U2, U3–U6, R1–R18, C1–C10) is Bolle's netlist from
MM Performer.sch, TheRealBolle/Performer-SE-PL-CL (CC-BY-NC-SA), adapted:
- SE only: 68000 DIP64 (IC1). Classic PLCC socket, U7 and SJ2 removed;
  C16M comes straight from PDS A29 (SJ2 closed equivalent).
- FPU clock tied to CLK_30 (SJ1 closed equivalent; QQ1 omitted).
- 68030 /CIOUT and /CBREQ brought out to P2 and U8 (unused on Bolle's board).

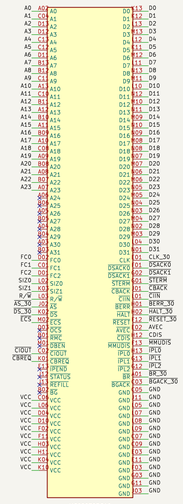
Populate GALs U3–U6 OR CPLD U8, never both. U8 is on all GAL bus nets;
GAL-to-GAL internal nets stay GAL-only. U8 pin assignment is a first pass.
U8 extras (DS, DSACK0, STERM, CBREQ, CBACK, CIOUT, ECS, HALT, BR, BGACK,
MMUDIS, IPL0/1, A1, RAMCARD, SPARE1/2) are for memory/cache experiments.

P2 per 261126-PigPen-P2-Memory-Port-Experimental-R2.

OPEN QUESTIONS:

1. P2.A17 is a U4 output (pin 13) with R4 pull-up; P2 sheet calls it an input.
2. RAMCARD sense: R19 pull-up = 'no card' is a guess.
3. Power corner: TPS2121 pin numbers are placeholders; R22–R24, C20 TBD
   from the datasheet. +5V_PDS = IN1 (priority), USB = IN2, OUT = VCC.
4. U8 dedicated inputs 1 and 84 tied to GND; JTAG pull-ups via fitter.

U1



MC68030RC16

68030 CPU, PGA120 socket

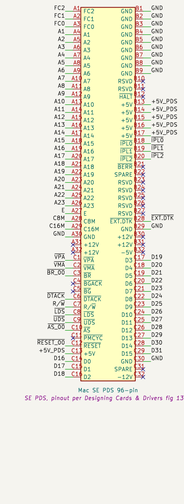
U2



MC68882FN16

FPU, PLCC68 socket. Clocked from CLK_30

J1



Mac SE PDS 96-pin

SE PDS, pinout per Designing Cards & Drivers fig 13-1

U8


GND CBM A23 A22 A21 A20 A19 A18 A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0 D31 D30 D29 D28 D27 D26 D25 D24 D23 D22 D21 D20 D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0 GND
IN/GCLR IN/OE1 IN/OE2/GCLK2 VCCINT I/O I/O I/O