Pig Pen J5: GAL Daughtercard Header

Pin assignment rev 0 (261126). 2x25, 1.27 mm (0.050 in) pitch. Main board J5 = vertical male header; GAL card J1 = vertical female socket on the card underside.
Pin 1 end = CPU end. Dir is from the GAL card: Out = a GAL drives it, In = the GAL card only reads it.

Row A (odd pins)

Pin	Signal	Dir	GAL pins | main board
1	**VCC**	Pwr	
3	**GND**	Gnd	
5	**CLK_30**	Out	U6.19 | 030, FPU, P2
7	**GND**	Gnd	
9	**SIZ0**	In	U5.4 | 030, P2
11	**SIZ1**	In	U5.3 | 030, P2
13	**/DSACK1**	Out	U4.12 | 030, FPU, P2, R2 pull-up
15	**/RESET_30**	Out	U5.13 U4.9 U6.8 | 030, FPU, P2, R3 pull-up
17	**/CIIN**	Out	U3.16 U5.7 | 030, P2
19	**/FPUCS**	Out	U3.18 U6.6 | FPU
21	**P2.A17**	Out	U4.13 | P2, R4 pull-up
23	**FC0**	In	U3.6 | 030, P2, PDS
25	**FC2**	In	U3.8 | 030, P2, PDS
27	**A19**	In	U3.5 | 030, P2, PDS
29	**A21**	In	U3.3 | 030, P2, PDS
31	**A23**	In	U3.1 | 030, P2, PDS
33	**/AS_00**	Out	U4.18 U5.2 U6.4 | PDS
35	**/LDS**	Out	U5.19 | PDS
37	**/VPA**	In	U4.6 | PDS
39	**E**	In	U4.7 U6.3 | P2, PDS
41	**GND**	Gnd	
43	**C16M**	In	U6.2 | PDS
45	**GND**	Gnd	
47	**/EXT.DTK**	Out	U3.13 | PDS, R16 pull-up
49	**VCC**	Pwr	

Row B (even pins)

Pin	Signal	Dir	GAL pins | main board
2	**VCC**	Pwr	
4	**A0**	In	U5.9 | 030, P2
6	**GND**	Gnd	
8	**SM_CLK16**	Out	U6.18 U4.1 | P2
10	**GND**	Gnd	
12	**/AS_30**	In	U4.4 U6.5 | 030, FPU, P2, R5 pull-up
14	**/BERR_30**	Out	U6.13 | 030, P2, R15 pull-up
16	**AVEC**	Out	U3.17 | 030
18	**CDIS**	Out	U6.14 | 030, R11 pull-up
20	**FPUSENSE**	In	U6.7 | FPU, R10 pull-up
22	**R/W**	In	U4.8 U5.5 | 030, FPU, P2, PDS
24	**FC1**	In	U3.7 | 030, P2, PDS
26	**GND**	Gnd	
28	**A20**	In	U3.4 | 030, P2, PDS
30	**A22**	In	U3.2 U5.8 | 030, P2, PDS
32	**/IPL2**	In	U5.6 | 030, PDS
34	**/UDS**	Out	U5.18 | PDS
36	**/DTACK**	In	U3.9 | PDS
38	**/VMA**	Out	U4.16 | PDS
40	**/BR_00**	Out	U5.16 | PDS
42	**/RESET_00**	Out	U5.12 | PDS
44	**GND**	Gnd	
46	**C8M**	In	U4.3 U5.1 U6.1 | PDS
48	**GND**	Gnd	
50	**VCC**	Pwr	

68030 side | 68000 / PDS side | Shared bus | FPU / P2 | Clock | +5V | GND

J5 GAL Daughtercard Header: Notes

Companion to 261126-PigPen-Main-Draft02 and 261126-PigPen-GAL-Card-Draft01 (KiCad).

What moved

- GALs U3, U4, U5, U6 and R9 (P3.B10 pull-up) move from the main board to the GAL card, wired exactly as on Bolle's MM Performer.sch (TheRealBolle/Performer-SE-PL-CL). U7 is not used on the SE.
- Six nets never leave the card: NOFC, U4_O1, U4_OE, /DTACK_SYS+EX, /SCC.RW.DEC, P3.B10.
- All other pull-ups stay on the main board (R2, R3, R4, R5, R10, R11, R15, R16), so the bus idles correctly with the card unplugged.
- The card carries one 100 nF cap per GAL plus a bulk cap.

Counts

- 37 signals + 4 VCC + 9 GND = 50 pins.
- 17 card outputs, 20 card inputs.
- SM_CLK16 and P2.A17 are GAL-only on Bolle's board but run to P2 on the Pig Pen, so they cross J5.

Layout of the pinout

- Pin 1 end (toward the CPU): CLK_30 and SM_CLK16, then the 68030-side signals, FPU and P2.
- Middle: the shared bus (R/W, FC0-FC2, A19-A23, /IPL2).
- Far end (toward the PDS): 68000-side signals, then C16M and C8M.
- Each clock has GND on every adjacent pin, along the row and across.
- VCC pairs at both ends (pins 1, 2, 49, 50).

Rules

- GAL card OR CPLD U8, never both. The fang next to J1 blocks the CPLD socket. Test-fit once with a CPLD seated.
- CPLD U8 is wired to every J5 signal, so either one can run the board.
- GAL card is for the bench only (vertical, or flat open-air). Inside a closed SE, use the CPLD.
- Power: four GAL16V8-15s draw roughly 0.4 A; four VCC pins at about 1 A each are ample.

Checks before committing

- Stack height of the header/socket pair, set from the cardboard mock-up.
- Pin 1 lines up with pin 1 after the 180-degree spin: place the card's socket footprint on the bottom layer (KiCad flips it) and confirm against the header drawing.
- 1.27 mm connectors grip less than 0.1 in: give the card a standoff at its far end.
- Keep the clock pins' traces short on both boards; CLK_30 runs from U6 on the card to the 68030 and FPU.