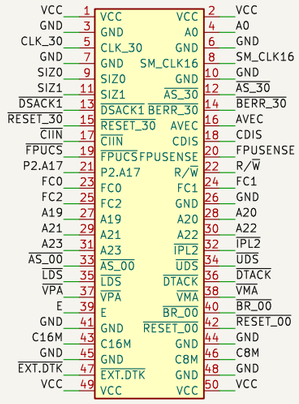
Pig Pen GAL daughtercard

BEST-GUESS DRAFT 0.1 (261126). jt Trash80 / FPD clone / Pig Pen

U3-U6 and R9 exactly as on Bolle's MM Performer.sch
(TheRealBolle/Performer-SE-PL-CL, CC-BY-NC-SA). U7 not used on the SE.
Card-only nets: NOFC, U4_O1, U4_OE, ~~DTACK_SYS+EX~~, ~~SCC.RW.DEC~~, P3.B10.
Everything else crosses J1 (see 261126-PigPen-GAL-Card-Header-R0).
C1-C4: one 100nF per GAL at its VCC pin. C5: bulk.

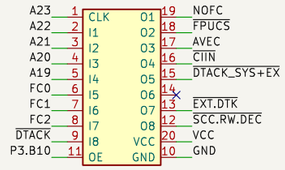
GAL card: bench only (vertical or open-air flat).
Inside a closed SE use the CPLD instead.
Fang next to J1 blocks the CPLD socket: GAL card OR CPLD, never both.

J1



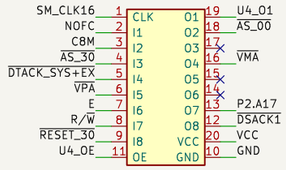
Mating socket 2x25 1.27mm (on card underside)
Mates with main-board J5, pin 1 to pin 1

U3



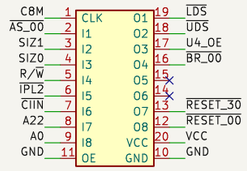
GAL16V8-15 / PALCE16V8-15
Bolle U3 (Micromac_Performer_U3.jed)

U4



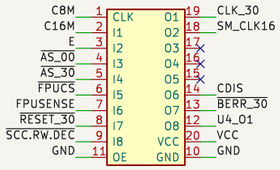
GAL16V8-15 / PALCE16V8-15
Bolle U4 (Micromac_Performer_U4.jed)

U5

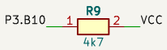


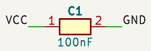
GAL16V8-15 / PALCE16V8-15
Bolle U5 (Micromac_Performer_U5.jed)

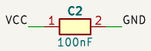
U6

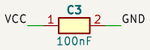


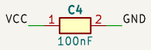
GAL16V8-15 / PALCE16V8-15
Bolle U6 (Micromac_Performer_U6.jed)

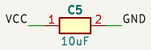












Plugs onto main-board J5. Bench use only
Performer core after Bolle, TheRealBolle/Performer-SE-PL-CL (CC-BY-NC-SA)
jt Trash80

Sheet: /
File: 261126-PigPen-GAL-Card-Draft01.kicad_sch

Title: Pig Pen GAL daughtercard (4x GAL16V8)

Size: A3	Date: 2026-11-26	**Rev: draft 0.1 best guess**
KiCad E.D.A. kicad-cli 7.0.11+dfsg-1build4		Id: 1/1