Pig Pen P2: Generic Memory Port

EXPERIMENTAL pin assignment, rev 0.2 (261126). 2x50, 1.27 mm (0.050 in) pitch, right-angle header + mating right-angle socket.
Pin assignment unchanged from rev 0 (261123). Rev 0.2 changes the notes only. Direction is from the Pig Pen.

Row A (odd pins)

Pin	Signal	Dir	Note
1	**+5V**	Pwr	
3	**D0**	I/O	
5	**D2**	I/O	
7	**D4**	I/O	
9	**D6**	I/O	
11	**GND**	Gnd	
13	**D8**	I/O	
15	**D10**	I/O	
17	**D12**	I/O	
19	**D14**	I/O	
21	**GND**	Gnd	
23	**D16**	I/O	
25	**D18**	I/O	
27	**D20**	I/O	
29	**D22**	I/O	
31	**GND**	Gnd	
33	**D24**	I/O	
35	**D26**	I/O	
37	**D28**	I/O	
39	**D30**	I/O	
41	**GND**	Gnd	
43	**R/W**	Out	
45	**/DS**	Out	
47	**SIZ0**	Out	
49	**FC0**	Out	
51	**FC2**	Out	
53	**/DSACK0**	In	Open drain, pulled up on Pig Pen
55	**P2.A17**	In	Card handshake (4.7K pull-up)
57	**GND**	Gnd	
59	**CLK_30**	Out	16 MHz CPU clock, GND all round
61	**GND**	Gnd	
63	**GND**	Gnd	
65	**/RESET**	Out	Buffered system reset
67	**/STERM**	In	4.7K pull-up on Pig Pen
69	**/CBREQ**	Out	From 68030
71	**/CIOUT**	Out	From 68030
73	**SPARE2**	n/c	Reserved
75	**A0**	Out	
77	**A2**	Out	
79	**A4**	Out	
81	**A6**	Out	
83	**+5V**	Pwr	
85	**A8**	Out	
87	**A10**	Out	
89	**A12**	Out	
91	**A14**	Out	
93	**A16**	Out	
95	**A18**	Out	
97	**A20**	Out	
99	**A22**	Out	

Row B (even pins)

Pin	Signal	Dir	Note
2	**+5V**	Pwr	
4	**D1**	I/O	
6	**D3**	I/O	
8	**D5**	I/O	
10	**D7**	I/O	
12	**GND**	Gnd	
14	**D9**	I/O	
16	**D11**	I/O	
18	**D13**	I/O	
20	**D15**	I/O	
22	**GND**	Gnd	
24	**D17**	I/O	
26	**D19**	I/O	
28	**D21**	I/O	
30	**D23**	I/O	
32	**GND**	Gnd	
34	**D25**	I/O	
36	**D27**	I/O	
38	**D29**	I/O	
40	**D31**	I/O	
42	**GND**	Gnd	
44	**/AS_30**	Out	
46	**ECS**	Out	
48	**SIZ1**	Out	
50	**FC1**	Out	
52	**RAMCARD**	In	Card fitted / select
54	**/DSACK1**	In	Open drain, pulled up on Pig Pen
56	**E**	Out	6800 E clock
58	**GND**	Gnd	
60	**GND**	Gnd	
62	**SM_CLK16**	Out	Host 16 MHz, GND all round
64	**GND**	Gnd	
66	**/BERR**	In	4.7K pull-up on Pig Pen
68	**/CIIN**	Out	GAL-driven: card monitors only
70	**/CBACK**	In	4.7K pull-up on Pig Pen
72	**SPARE1**	n/c	Reserved
74	**GND**	Gnd	
76	**A1**	Out	
78	**A3**	Out	
80	**A5**	Out	
82	**A7**	Out	
84	**+5V**	Pwr	
86	**A9**	Out	
88	**A11**	Out	
90	**A13**	Out	
92	**A15**	Out	
94	**A17**	Out	
96	**A19**	Out	
98	**A21**	Out	
100	**A23**	Out	

Data · Address · Control · Clock · Cache superset (new) · Spare · +5V · GND

P2 Memory Port: Notes

Rev 0.2 (261126): status notes reworded; pin assignment and connector unchanged from rev 0.1.

Status

- Experimental. The pin order is new; it is not the original Total Systems Mercury P2 layout.
- Signal set adapted and extended from Bolle's published Performer schematic (TheRealBolle/Performer-SE-PL-CL).
- RAM boards built to other P2 layouts need an adapter or respin to use this port.
- If the original P2 layout turns up, revisit before the board is released.

Connector

- 2x50 at 1.27 mm (0.050 in) pitch: right-angle male header on the Pig Pen, mating right-angle female socket on the card, so the card sits level with the Pig Pen and extends toward the front.
- Length: about 62 mm of pins, about 66 mm with the housing ends. Fits the 10 cm board edge with ~30 mm to spare (0.1 in would be ~127 mm; 2 mm ~100 mm of pins, too long once the housing is added).
- Right-angle pairs flip rows A/B like turning a page. Confirm pin 1 and row A/B on both parts' drawings before finalizing, so the card isn't mirrored.
- Current: ~1 A per pin at 1.27 mm; the four +5V pins are ample within the SE PDS budget.
- Through-hole, hand-soldered at assembly. Finer pins than 0.1 in: a fine soldering tip helps.
- 1.27 mm connectors grip less than 0.1 in: the card needs a standoff or foot at its far end.

Counts

- 81 signals + 15 GND + 4 +5V = 100 pins.
- Data D0-D31 (32), Address A0-A23 (24), Control 15, Clocks 2, Cache 6, Spare 2.
- Data: a GND row every 8 bits. Each clock has GND on all adjacent pins (along and across).

Base RAM-card signals (from Bolle's published schematic)

- A0-A23, D0-D31, RAMCARD, FC0, FC1, SIZ0, SIZ1, R/W, /AS_30, ECS,
- SM_CLK16, CLK_30, E, P2.A17, /DSACK0, /DSACK1.

Added for the superset

- FC2, /DS, /RESET: full function code, data strobe, and a clean reset for the card.
- /STERM: synchronous 32-bit termination, for zero-wait-state cache or fast SRAM.
- /CBREQ, /CBACK: 68030 burst fill (cache line fills, SN74ACT2155-style card).
- /CIIN: Pig Pen GAL already drives it (no caching for I/O); card watches it only.
- /CIOUT: 68030 output telling an external cache not to cache this cycle.
- /BERR: lets a card end a bad cycle; pulled up on the Pig Pen.
- SPARE1, SPARE2: unconnected on rev 0, reserved for whatever comes next.

Pig Pen side (with no card fitted)

- 4.7K pull-ups on /STERM, /CBACK, /BERR, /DSACK0, /DSACK1, P2.A17 so the CPU runs normally.
- RAMCARD default must read "no card"; check its sense against the U3-U6 GAL logic.
- Header holes only on the release board (provision, like the FPU osc and SJ1).

Checks before committing

- Pick the right-angle header/socket pair and confirm the row flip on their drawings.
- Power: the whole card shares the SE PDS budget (1.5 A at +5V, 7 W).
- Card envelope: the level card must stay within the SE PDS card outline at the front, and its parts within the 15.58 mm rear / 4.61 mm front height limits.
- 24-bit address only (A0-A23), as the SE is a 24-bit machine.