

IDT71B74

- High-speed address to MATCH comparison time
 - Commercial: 8/10/12/15/20ns (max.)
- High-speed address access time
 - Commercial: 8/10/12/15/20ns (max.)
- High-speed chip select access time
 - Commercial: 6/7/8/10ns (max.)
- Power-ON Reset Capability
- Low power consumption
 - 830mW (typ.) for 12ns parts
 - 880mW (typ.) for 10ns parts
 - 920mW (typ.) for 8ns parts
- Produced with advanced BiCMOS high-performance technology
- Input and output directly TTL-compatible
- Standard 28-pin plastic DIP and 28-pin SOJ (300 mil)

The IDT71B74 is a high-speed cache address comparator subsystem consisting of a 65,536-bit static RAM organized as 8K x 8 and an 8-bit comparator. A single IDT71B74 can map 8K cache words into a 2 megabyte address space by using the 21 bits of address organized with the 13 LSBs for the cache address bits and the 8 higher bits for cache data bits. Two IDT71B74s can be combined to provide 29 bits of address comparison, etc. The IDT71B74 also provides a single RAM clear control, which clears all words in the internal RAM to zero when activated. This allows the tag bits for all locations to be cleared at power-on or system-reset, a requirement for cache comparator systems. The IDT71B74 can also be used as a resettable 8K x 8 high-speed static RAM.

The MATCH pin of several IDT71B74s can be wired-ORed together to provide enabling or acknowledging signals to the data cache or processor, thus eliminating logic delays and increasing system throughput.

The block diagram illustrates the internal architecture of the 65536-bit memory array system. It includes the following components and connections:

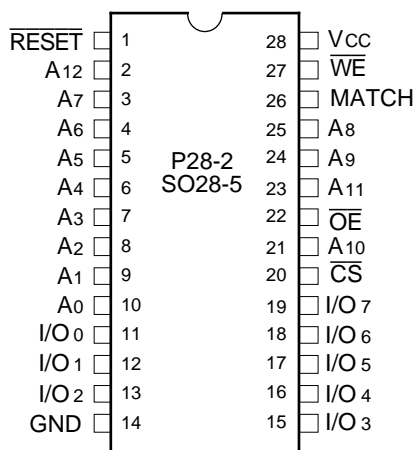
- Inputs:** Address lines A_0 through A_{12} , a $\overline{\text{RESET}}$ signal, an 8-bit $\text{I/O}_0 - 7$ bus, and control signals $\overline{\text{WE}}$, $\overline{\text{OE}}$, and $\overline{\text{CS}}$.
- ADDRESS DECODER:** Receives address lines A_0 through A_{12} and provides a 13-bit output to the memory array.
- 65,536-BIT MEMORY ARRAY:** Receives the 13-bit address from the decoder and provides a 16-bit data output to the I/O control block.
- I/O CONTROL:** Receives the 8-bit $\text{I/O}_0 - 7$ bus and the 16-bit data from the memory array. It also receives $\overline{\text{WE}}$ and $\overline{\text{OE}}$ signals and provides a $\overline{\text{MATCH}}$ output.
- CONTROL LOGIC:** Receives $\overline{\text{WE}}$, $\overline{\text{OE}}$, and $\overline{\text{CS}}$ signals. It provides control signals to the ADDRESS DECODER and the I/O CONTROL block.
- EQUAL:** A comparator that receives the 16-bit data from the memory array and the 16-bit data from the I/O control block. It provides a $\overline{\text{MATCH}}$ output.
- MATCH (OPEN DRAIN):** The final output of the system, which is the logical AND of the $\overline{\text{MATCH}}$ signals from the I/O control block and the EQUAL comparator.

3013 drw 01

AUGUST 1996

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PIN CONFIGURATION



DIP/SOJ
TOP VIEW

3013 drw 02

TRUTH TABLE^(1, 2)

\overline{WE}	\overline{CS}	\overline{OE}	RESET	MATCH	I/O	Function
X	X	X	L	HIGH	—	Reset all bits to LOW
X	H	X	H	HIGH	Hi-Z	Deselect chip
H	L	H	H	LOW	DIN	No MATCH
H	L	H	H	HIGH	DIN	MATCH
H	L	L	H	HIGH	DOUT	Read
L	L	X	H	HIGH	DIN	Write

NOTES:

1. H = V_{IH} , L = V_{IL} , X = DON'T CARE
2. HIGH = High-Z (pulled up by an external resistor), and LOW = V_{OL} .

3013 tbl 01

PIN DESCRIPTIONS

Pin Names	Description
A0-12	Address
I/O0-7	Data Input/Output
\overline{CS}	Chip Select
RESET	Memory Reset
MATCH	Data/Memory Match (Open Drain)
\overline{WE}	Write Enable
\overline{OE}	Output Enable
GND	Ground
Vcc	Power

3013 tbl 02

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Com'l.	Unit
$V_{TERM}^{(2)}$	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed $V_{CC} + 0.5V$.

3013 tbl 03

CAPACITANCE

($T_A = +25^\circ\text{C}$, $f = 1.0\text{MHz}$, SOJ Package)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 3dV$	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 3dV$	7	pF

NOTE:

1. This parameter is determined by device characterization, but is not production tested.

3013 tbl 04

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V _{IH}	Input HIGH Voltage ⁽¹⁾	2.2	—	6.0 ⁽⁴⁾	V
V _{IHR}	$\overline{\text{RESET}}$ Input Voltage	2.5 ⁽²⁾	—	6.0	V
V _{IL}	Input LOW Voltage	−0.5 ⁽³⁾	—	0.8	V

NOTES:

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- All inputs except $\overline{\text{RESET}}$.
- When using bipolar devices to drive the $\overline{\text{RESET}}$ input, a pullup resistor of 1k Ω –10k Ω is usually required to assure this voltage.
- V_{IL} (min.) = −1.5V for pulse width less than 10ns, once per cycle.
- V_{TERM} must not exceed V_{CC} + 0.5V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	V _{CC}
Commercial	0°C to +70°C	0V	5V \pm 10%

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DC ELECTRICAL CHARACTERISTICS⁽¹⁾

(V_{CC} = 5.0V \pm 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} − 0.2V)

Symbol	Parameter		71B74S8	71B74S10	71B74S12	71B74S15	71B74S20	Unit
I _{CC}	Dynamic Operating Current Outputs Open, V _{CC} = Max., f = f _{MAX} ⁽²⁾	$\overline{\text{WE}}$ = V _{LC}	230	210	200	190	180	mA
		$\overline{\text{WE}}$ = V _{HC}	210	200	170	160	150	mA

NOTES:

3013 tbl 07

- All values are maximum guaranteed values.
- f_{MAX} = 1/t_{RC}, only input addresses are cycling at f_{MAX}.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE (V_{CC} = 5.0V \pm 10%)

Symbol	Parameter	Test Condition	IDT71B74S		Unit
			Min.	Max.	
I _{LI}	Input Leakage Current	V _{CC} = Max., V _{IN} = GND to V _{CC}	—	5	μ A
I _{LO}	Output Leakage Current	V _{CC} = Max., $\overline{\text{CS}}$ = V _{IH} , V _{OUT} = GND to V _{CC}	—	5	μ A
V _{OL}	Output LOW Voltage	I _{OL} = 22mA MATCH	—	0.5	V
		I _{OL} = 18mA MATCH	—	0.4	
		I _{OL} = 10mA, V _{CC} = Min. (Except MATCH)	—	0.5	
		I _{OL} = 8mA, V _{CC} = Min. (Except MATCH)	—	0.4	
V _{OH}	Output HIGH Voltage	I _{OH} = −4mA, V _{CC} = Min. (Except MATCH)	2.4	—	V

3013 tbl 08

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1, 2, and 3

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Figure 1. AC Test Load

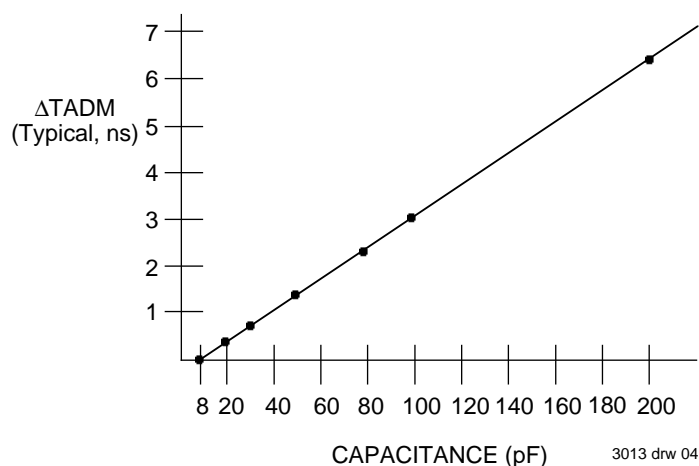


Figure 1A. Lumped Capacitive Load
Typical Derating Curve

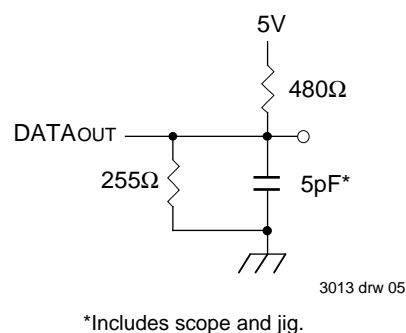


Figure 2. AC Test Load
(for tCLZ, tOLZ, tCHZ, tOHZ, tOW, tWHZ)

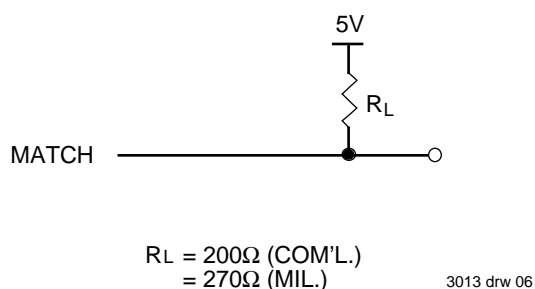


Figure 3. AC Test Load for MATCH

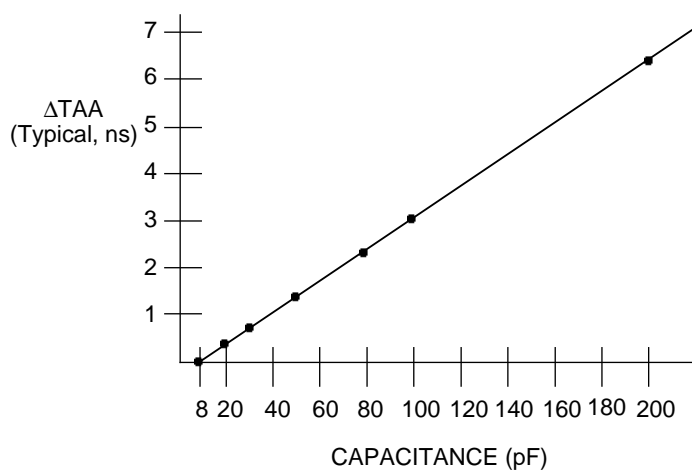
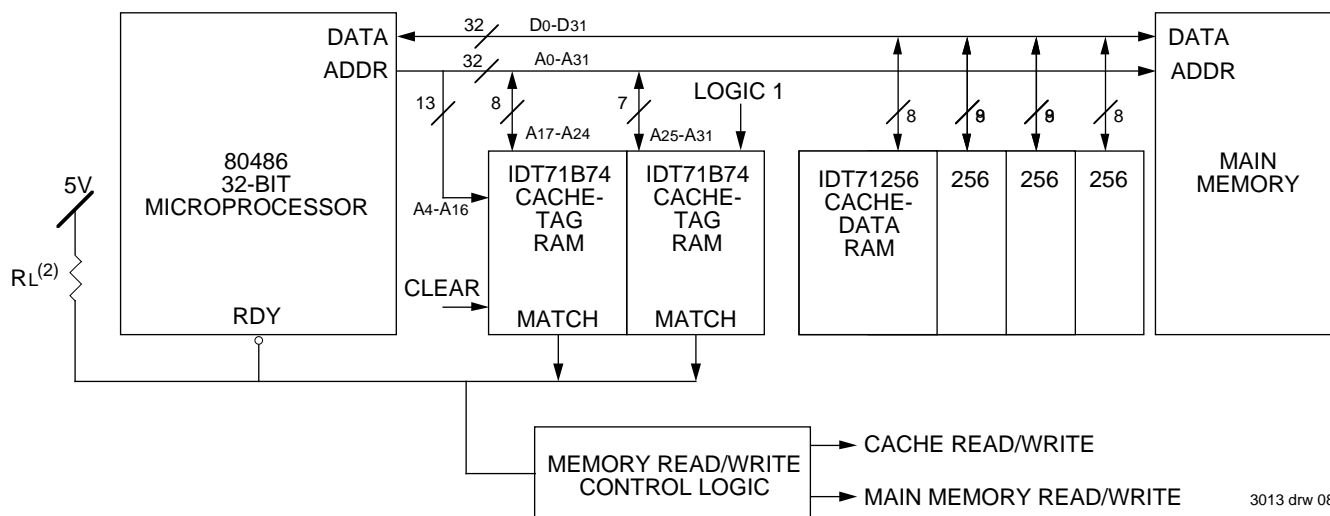


Figure 3A. Lumped Capacitive Load
Typical Derating Curve



NOTES:

- For more information refer to IDT Application Notes AN-07 and AN-78 and Technical Notes TN-11 and TN-13.
- $R_L = 200\Omega$.

Figure 4. Example of Cache Memory System Block Diagram

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%)

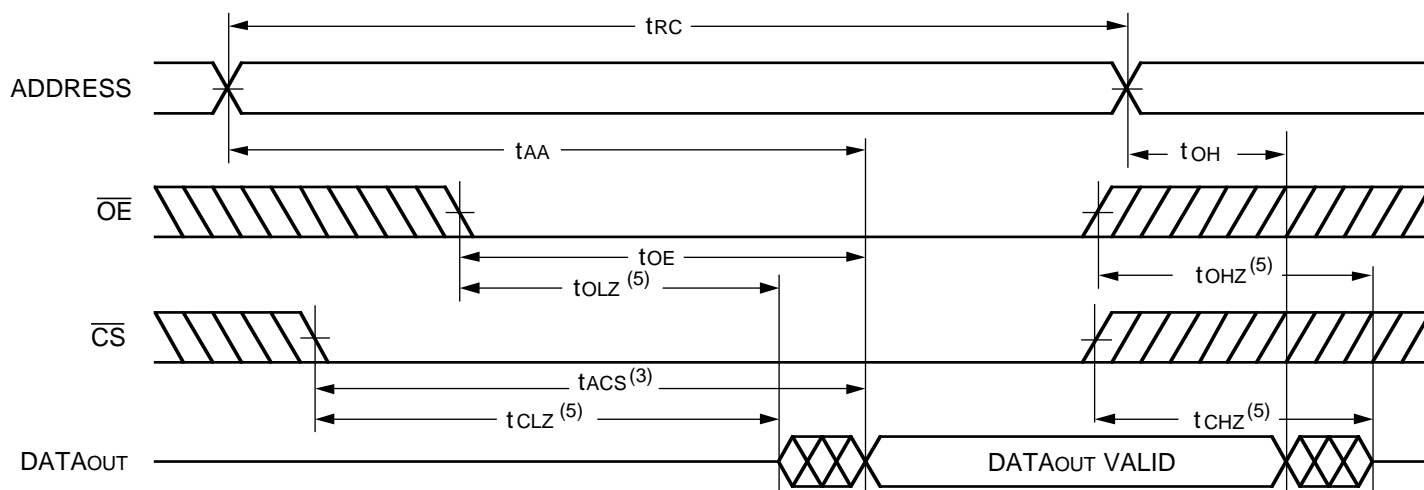
Symbol	Parameter	71B74S8		71B74S10		71B74S12		71B74S15		71B74S20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
tRC	Read Cycle Time	8	—	10	—	12	—	15	—	20	—	ns
tAA	Address Access Time	—	8	—	10	—	12	—	15	—	20	ns
tACS	Chip Select Access Time	—	6	—	7	—	8	—	8	—	10	ns
tCLZ ⁽¹⁾	Chip Select to Output in Low-Z	2	—	2	—	2	—	3	—	3	—	ns
tOE	Output Enable to Output Valid	—	5	—	6	—	6	—	8	—	9	ns
tOLZ ⁽¹⁾	Output Enable to Output in Low-Z	2	—	2	—	2	—	2	—	2	—	ns
tCHZ ⁽¹⁾	Chip Select to Output in High-Z	—	4	—	5	—	5	—	7	—	8	ns
tOHZ ⁽¹⁾	Output Disable to Output in High-Z	—	4	—	4	—	5	—	5	—	8	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	3	—	3	—	ns

NOTE:

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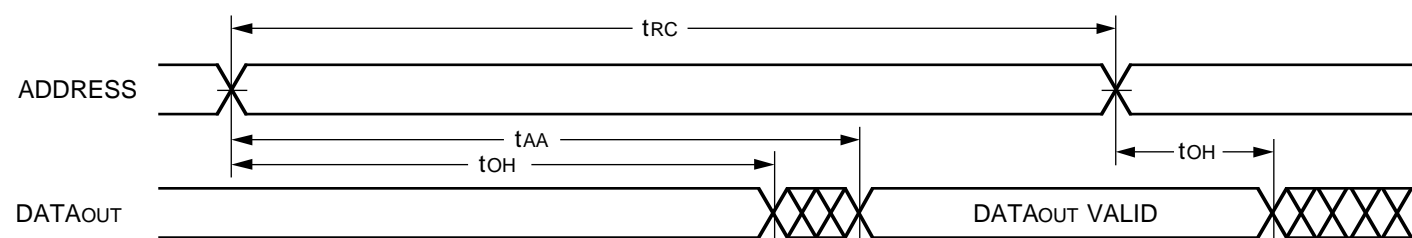
1. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.

TIMING WAVEFORM OF READ CYCLE NO. 1⁽¹⁾



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TIMING WAVEFORM OF READ CYCLE NO. 2^(1, 2, 4)



NOTES:

3013 drw 10

1. WE is HIGH for Read cycle.
2. Device is continuously selected, CS is LOW.
3. Address valid prior to or coincident with CS transition LOW; otherwise t_{AA} is the limiting parameter.
4. OE is continuously active, OE is LOW.
5. Transition is measured ±200mV from steady state.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%)

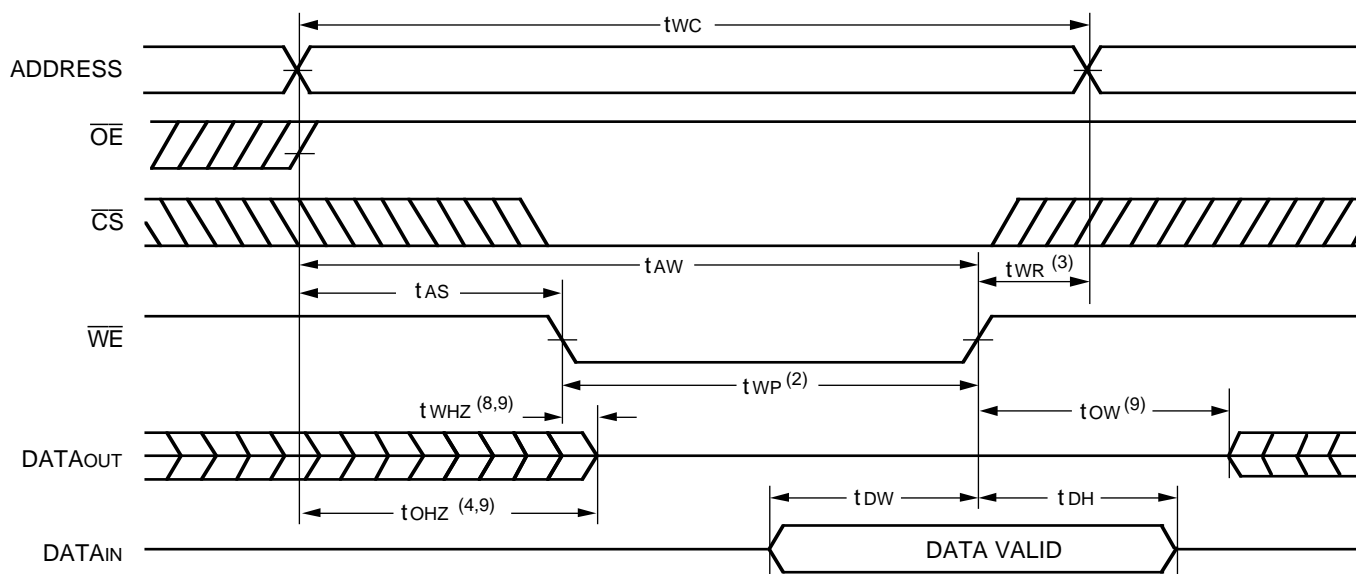
Symbol	Parameter	71B74S8		71B74S10		71B74S12		71B74S15		71B74S20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle												
tWC	Write Cycle Time	8	—	10	—	12	—	15	—	20	—	ns
tCW	Chip Select to End of Write	7	—	8	—	9	—	10	—	15	—	ns
tAW	Address Valid to End of Write	7	—	8	—	9	—	10	—	15	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	7	—	8	—	9	—	10	—	15	—	ns
tWR	Write Recovery Time ($\overline{\text{CS}}$, $\overline{\text{WE}}$)	0	—	0	—	0	—	0	—	0	—	ns
tWHZ ⁽¹⁾	Write Enable to Output in High-Z	—	5	—	5	—	5	—	5	—	5	ns
tDW	Data Valid to End of Write	5	—	5	—	6	—	8	—	10	—	ns
tDH	Data Hold from Write Time	0	—	0	—	0	—	0	—	0	—	ns
tOW ⁽¹⁾	Output Active from End of Write	2	—	2	—	2	—	2	—	2	—	ns

NOTE:

3013 tbl 11

1. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{\text{WE}}$ Controlled Timing, $\overline{\text{OE}}$ HIGH During Write)^(1, 6)

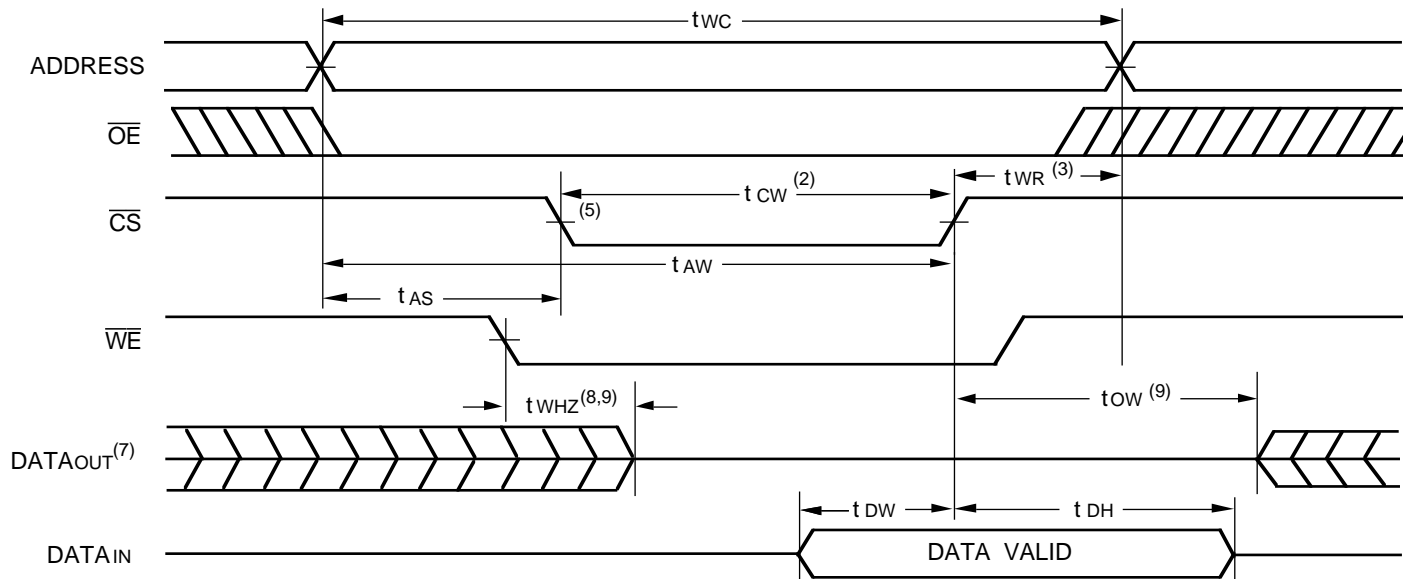


NOTES:

3013 drw 11

1. $\overline{\text{WE}}$, $\overline{\text{CS}}$ must be inactive during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{\text{WE}}$ and a LOW $\overline{\text{CS}}$.
3. t_{WR} is measured from the earlier of $\overline{\text{CS}}$ or $\overline{\text{WE}}$ going HIGH to the end of the write cycle.
4. During this period, I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{\text{CS}}$ LOW transition occurs simultaneously with or after the $\overline{\text{WE}}$ LOW transition, the outputs remain in a high-impedance state.
6. $\overline{\text{OE}}$ is continuously HIGH, $\overline{\text{OE}} \geq V_{\text{IH}}$. If during the $\overline{\text{WE}}$ controlled write cycle the $\overline{\text{OE}}$ is LOW, t_{WP} must be greater or equal to $t_{\text{WHZ}} + t_{\text{DW}}$ to allow the I/O drivers to turn off and the data to be placed on the bus for the required t_{DW} . If $\overline{\text{OE}}$ is HIGH during the $\overline{\text{WE}}$ controlled write cycle, this requirement does not apply and the minimum write pulse is the specified t_{WP} . For a $\overline{\text{CS}}$ controlled write cycle, $\overline{\text{OE}}$ may be LOW with no degradation to t_{CW} timing.
7. DATA_{OUT} is never enabled, therefore the output is in High-Z state during the entire write cycle.
8. t_{WHZ} is not included if $\overline{\text{OE}}$ remains HIGH during the write cycle. If $\overline{\text{OE}}$ is LOW during the Write Enabled write cycle then t_{WHZ} must be added to t_{WP} and t_{CW} .
9. Transition is measured $\pm 200\text{mV}$ from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{\text{CS}}$ Controlled Timing)^(1, 6)



3013 drw 12

NOTES:

- $\overline{\text{WE}}$, $\overline{\text{CS}}$ must be inactive during all address transitions.
- A write occurs during the overlap of a LOW $\overline{\text{WE}}$ and a LOW $\overline{\text{CS}}$.
- t_{WR} is measured from the earlier of $\overline{\text{CS}}$ or $\overline{\text{WE}}$ going HIGH to the end of the write cycle.
- During this period, I/O pins are in the output state and input signals must not be applied.
- If the $\overline{\text{CS}}$ LOW transition occurs simultaneously with or after the $\overline{\text{WE}}$ LOW transition, the outputs remain in a high-impedance state.
- $\overline{\text{OE}}$ is continuously HIGH, $\overline{\text{OE}} \geq V_{\text{IH}}$. If during the $\overline{\text{WE}}$ controlled write cycle the $\overline{\text{OE}}$ is LOW, t_{WP} must be greater or equal to $t_{\text{WHZ}} + t_{\text{OW}}$ to allow the I/O drivers to turn off and the data to be placed on the bus for the required t_{DW} . If $\overline{\text{OE}}$ is HIGH during the $\overline{\text{WE}}$ controlled write cycle, this requirement does not apply and the minimum write pulse is the specified t_{WP} . For a $\overline{\text{CS}}$ controlled write cycle, $\overline{\text{OE}}$ may be LOW with no degradation to t_{CW} timing.
- $\text{DATAOUT}^{(7)}$ is never enabled, therefore the output is in High-Z state during the entire write cycle.
- t_{WHZ} is not included if $\overline{\text{OE}}$ remains HIGH during the write cycle. If $\overline{\text{OE}}$ is LOW during the Write Enabled write cycle then t_{WHZ} must be added to t_{WP} and t_{CW} .
- Transition is measured $\pm 200\text{mV}$ from steady state.

AC ELECTRICAL CHARACTERISTICS ($V_{\text{CC}} = 5.0\text{V} \pm 10\%$)

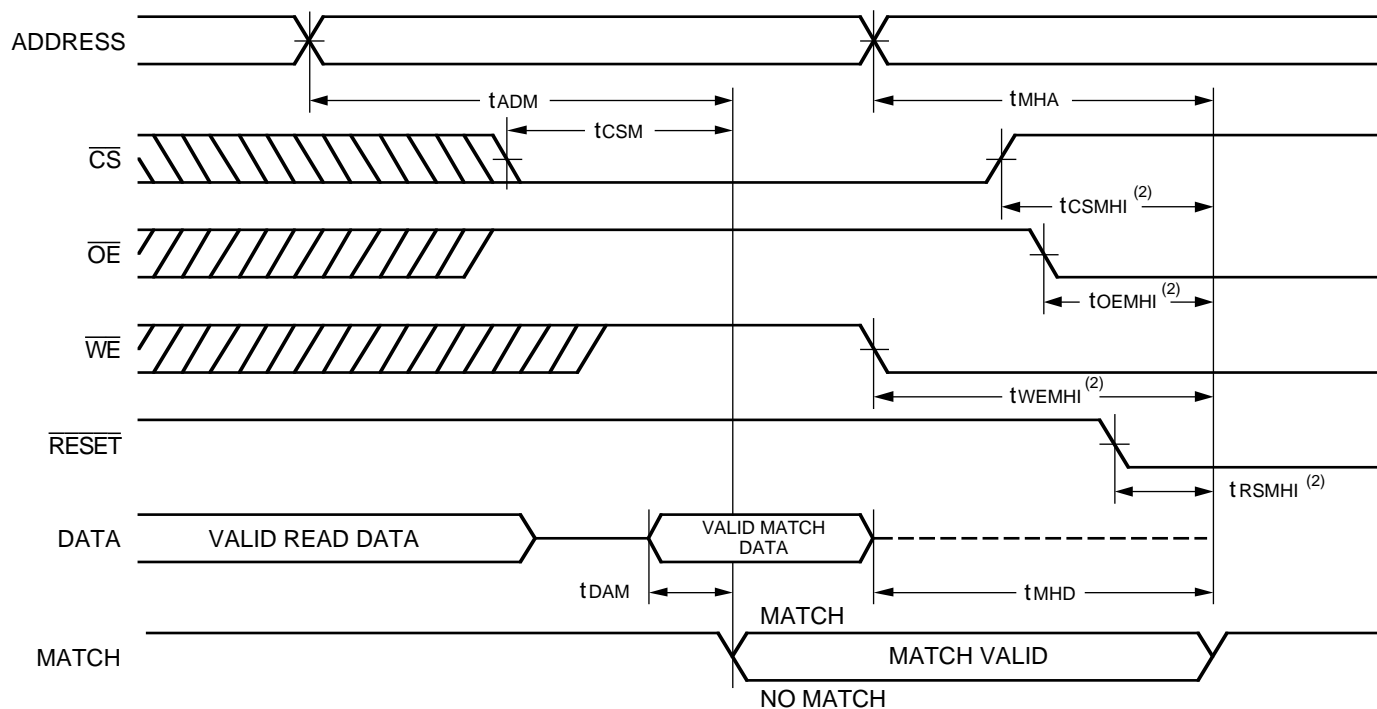
Symbol	Parameter	71B74S8		71B74S10		71B74S12		71B74S15		71B74S20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Match Cycle												
tADM	Address to MATCH Valid	—	8	—	10	—	12	—	15	—	20	ns
tCSM	Chip Select to MATCH Valid	—	7	—	7	—	8	—	10	—	10	ns
tCSMH ⁽¹⁾	Chip Select to MATCH HIGH	—	7	—	8	—	8	—	8	—	8	ns
tDAM	Data Input to MATCH Valid	—	7	—	8	—	10	—	12	—	12	ns
tOEMH ⁽¹⁾	$\overline{\text{OE}}$ LOW to MATCH HIGH	—	7	—	8	—	10	—	10	—	10	ns
tWEMH ⁽¹⁾	$\overline{\text{WE}}$ LOW to MATCH HIGH	—	7	—	8	—	10	—	10	—	10	ns
tRSMH ⁽¹⁾	$\overline{\text{RESET}}$ LOW to MATCH HIGH	—	8	—	10	—	10	—	12	—	15	ns
tMHA	MATCH Valid Hold From Address	2	—	2	—	2	—	2	—	2	—	ns
tMHD	MATCH Valid Hold From Data	2	—	2	—	2	—	2	—	2	—	ns

NOTE:

- This parameter is guaranteed with the AC Load (Figure 3) by device characterization, but is not production tested.

3013 tbl 12

MATCH TIMING⁽¹⁾



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NOTES:

1. It is not recommended to float data and address input pins while the MATCH pin is active.
2. Transition is measured at $\pm 200\text{mV}$ from steady state.

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0\text{V} \pm 10\%$)

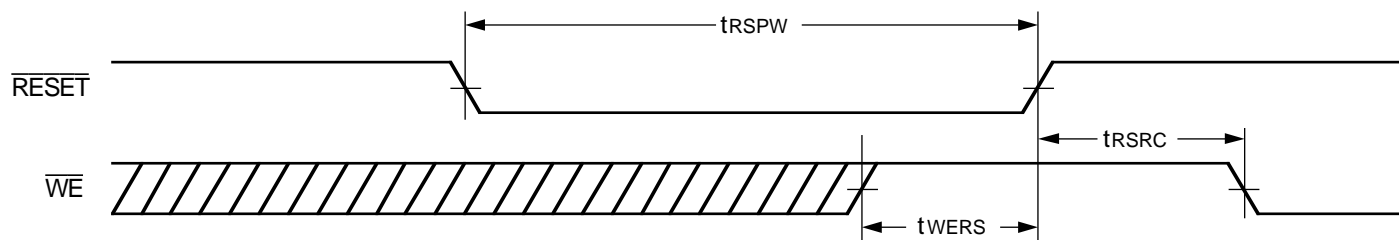
Symbol	Parameter	71B74S8		71B74S10		71B74S12		71B74S15		71B74S20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Reset Cycle												
trSPW ⁽¹⁾	Reset Pulse Width	30	—	35	—	35	—	40	—	45	—	ns
tWERS	\overline{WE} HIGH to Reset HIGH	5	—	5	—	5	—	5	—	5	—	ns
trSRC	Reset HIGH to \overline{WE} LOW	25	—	25	—	25	—	30	—	30	—	ns
tPORS ⁽²⁾	Power On Reset	100	—	100	—	100	—	120	—	120	—	ns

NOTES:

1. Recommended duty cycle = 10% maximum.
2. This parameter is guaranteed with the AC Load (Figure 1) by device characterization, but is not production tested.

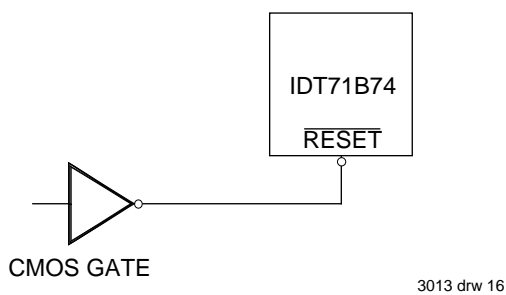
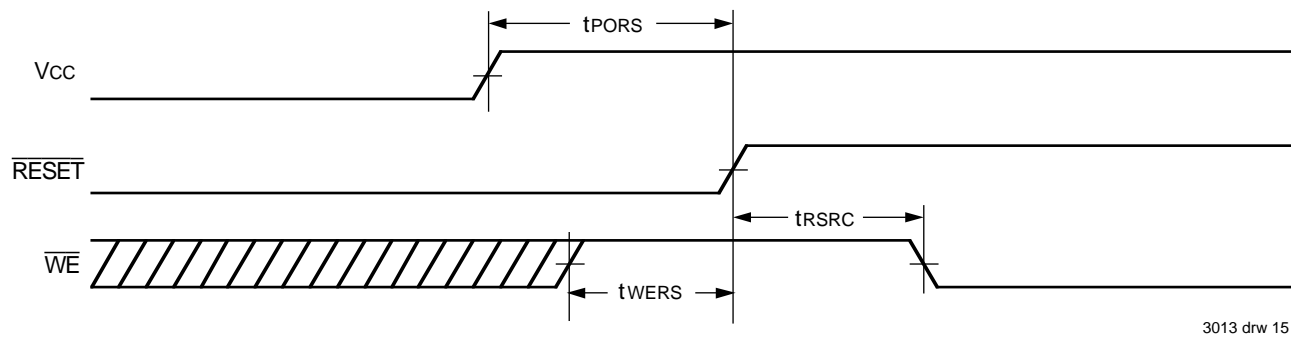
3013 tbl 13

RESET TIMING

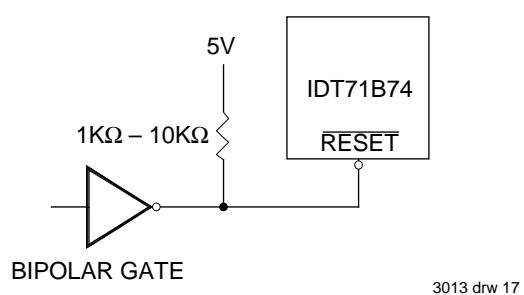


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POWER ON RESET TIMING



Driving the RESET pin with CMOS logic.



Driving the RESET pin with bipolar logic.

Figure 5.

ORDERING INFORMATION

IDT	71B74	S	XX	X	X		
Device Type	Power	Speed	Package	Process/ Temperature Range			
					Blank	Commercial (0°C to +70°C)	
					TP	Plastic DIP (300 mil) (P28-2)	
					Y	SOJ (Small Outline IC, J-bend) (SO28-5)	
					8	Commercial Only, SOJ Only	Speed in ns
					10	Commercial Only	
					12	Commercial Only	
					15	Commercial Only	
					20	Commercial Only	

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