L5380/53C80
SCSI Bus Controller

FEATURES

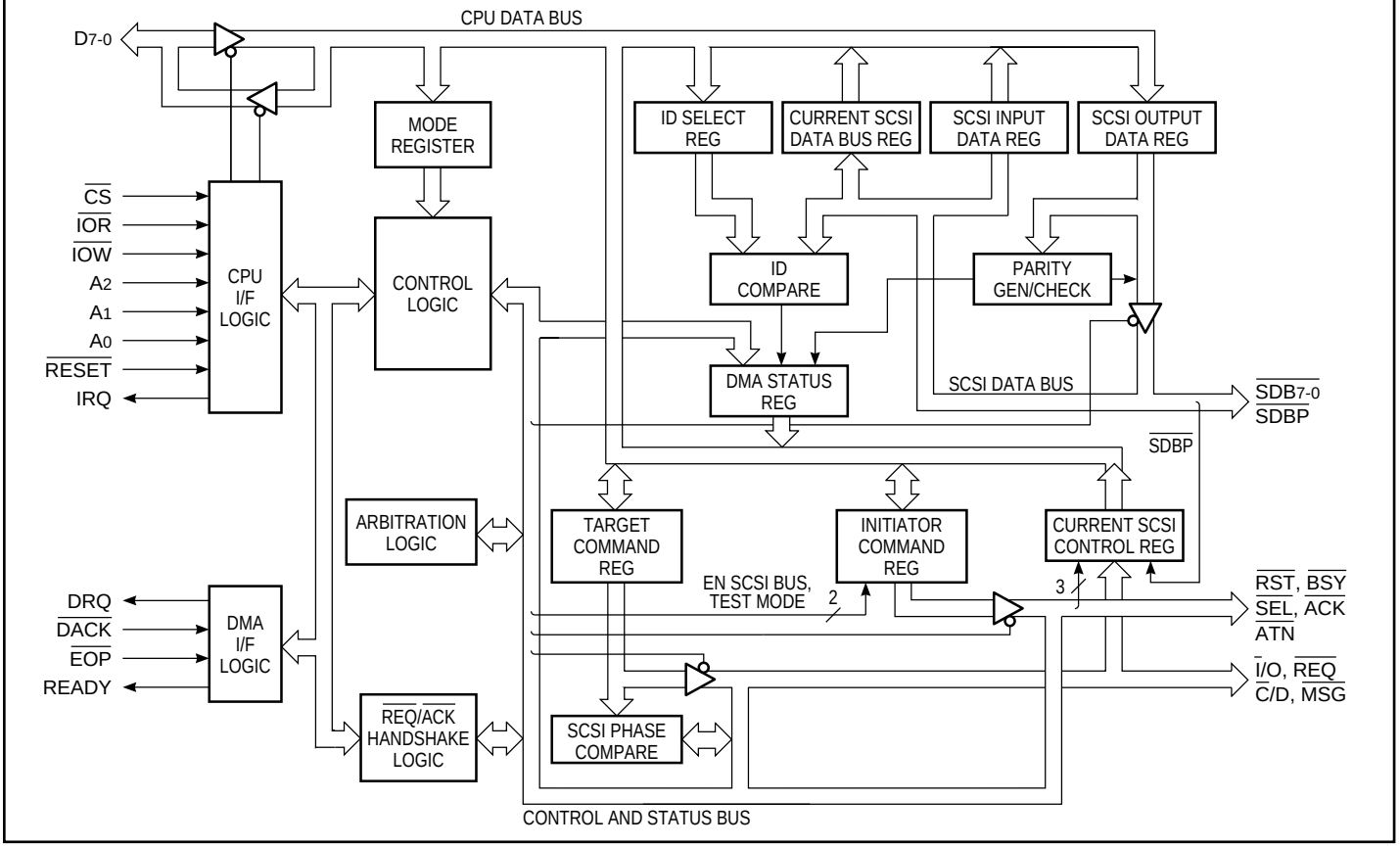
- Asynchronous Transfer Rate Up to 4 Mbytes/sec
- Low Power CMOS Technology
- Replaces NCR 5380/53C80/ 53C80-40 and AMD Am5380/ 53C80
- On-Chip SCSI Bus Drivers
- Supports Arbitration, Selection/ Reselection, Initiator or Target Roles
- Programmed or DMA I/O, Handshake or Wait State DMA Interlock
- DECC SMD No.
  5962-90548 — L53C80
- Package Styles Available:
  - 40/48-pin Plastic DIP
  - 48-pin Sidebraze, Hermetic DIP
  - 44-pin Plastic LCC, J-Lead

DESCRIPTION

The **L5380/53C80** are high performance SCSI bus controllers which support the physical layer of the SCSI (Small Computer System Interface) bus as defined by the ANSI X3T9.2 committee. It is pin and functionally compatible with the NMOS NCR5380, while offering up to a 2.5x performance improvement, 10x power reduction, and lower cost. Replacement of the NMOS 5380 by the LOGIC Devices L5380/53C80 will result in an immediate transfer rate improvement due to $\overline{REQ}/\overline{ACK}$ and $\overline{DRQ}/\overline{DACK}$ handshake response times up to 5 times faster than previous devices. While remaining firmware compatible with the NCR5380, the L5380/53C80 provides bug fixes and state machine enhancements allowing even larger throughput gains for new designs.

The L5380/53C80 supports asynchronous data transfer between initiator and target at up to 4 Mbytes/sec. It operates in either initiator or target roles and offers a choice of programmed I/O (direct microprocessor manipulation of handshake) or any of several DMA modes (autonomous handshake and data transfer operations). The L5380/53C80 has internal hardware to support arbitration and can monitor and generate interrupts for a variety of error conditions. It provides extensive bus status monitoring features and includes buffers capable of directly driving a terminated SCSI bus for a compact implementation.

L5380/53C80 BLOCK DIAGRAM



PIN DEFINITIONS

A. SCSI Bus

$\overline{SDB7–0}$ — SCSI DATA BUS 7–0

Bidirectional/Active low. The 8-bit SCSI data bus is defined by these pins. $\overline{SDB7}$ is the most significant bit. During arbitration phase, these lines contain the SCSI ID numbers of all initiators arbitrating for the SCSI bus; $\overline{SDB7}$ represents the initiator with the highest priority. During the selection/reselection phase, these lines contain the ID number of the device that won the arbitration along with the ID number of the device to be selected/reselected.

$\overline{SDBP}$ — SCSI DATA BUS PARITY

Bidirectional/Active low. $\overline{SDBP}$ is the parity bit of the SCSI data bus. Odd parity is used, meaning that the total number of ones on the bus, including the parity bit, is odd. Parity is always generated when sending information, however checking for parity errors when receiving information is a user option. Parity is not valid during arbitration phase.

$\overline{SEL}$ — SELECT

Bidirectional/Active low. $\overline{SEL}$ is asserted by the initiator to select a target. It is also asserted by the target when reselecting it as an initiator.

$\overline{BSY}$ — BUSY

Bidirectional/Active low. $\overline{BSY}$ is asserted to indicate that the SCSI bus is active.

$\overline{ACK}$ — ACKNOWLEDGE

Bidirectional/Active low. $\overline{ACK}$ is asserted by the initiator during any information transfer phase in response to assertion of $\overline{REQ}$ by the target. Similarly, $\overline{ACK}$ is deasserted after $\overline{REQ}$ becomes inactive. These two signals form the data transfer handshake between the initiator and target. Data is latched by the target on the lowgoing edge of $\overline{ACK}$ for target receive operations.

$\overline{ATN}$ — ATTENTION

Bidirectional/Active low. $\overline{ATN}$ is asserted by the initiator after successful selection of a target, to indicate an intention to send a message to the target. The target responds to $\overline{ATN}$ by entering the MESSAGE OUT phase.

$\overline{RST}$ — SCSI BUS RESET

Bidirectional/Active low. $\overline{RST}$ when active indicates a SCSI bus reset condition.

$\overline{I}$/O — INPUT/OUTPUT

Bidirectional/Active low. $\overline{I}$/O is controlled by the target and specifies the direction of information transfer. When $\overline{I}$/O is asserted, the direction of transfer is to the initiator. $\overline{I}$/O is also asserted by the target during RESELECTION phase to distinguish it from SELECTION phase.

$\overline{C}$/D — CONTROL/DATA

Bidirectional/Active low. $\overline{C}$/D is controlled by the target and when asserted, indicates CONTROL (command or status) information is on the SCSI data bus. DATA is specified when $\overline{C}$/D is deasserted.

$\overline{MSG}$ — MESSAGE

Bidirectional/Active low. $\overline{MSG}$ is controlled by the target, and when asserted indicates MESSAGE phase.

$\overline{REQ}$ — REQUEST

Bidirectional/Active low. $\overline{REQ}$ is asserted by the target to begin the handshake associated with transfer of a byte over the SCSI data bus. $\overline{REQ}$ is deasserted upon receipt of $\overline{ACK}$ from the initiator. Data is latched by the initiator on the lowgoing edge of $\overline{REQ}$ for initiator receive operations.

B. Microprocessor Bus

$\overline{CS}$ — CHIP SELECT

Input/Active low. This signal enables reading or writing of the internal registers by the microprocessor, using memory mapped I/O. An alternate method for reading selected registers is available for DMA.

DRQ — DMA REQUEST

Output/Active high. This signal is used to indicate that the L5380/53C80 is ready to execute the next cycle of a DMA transfer on the microprocessor bus. For send operations, it indicates that the output data register is ready to receive the next byte from the DMA controller or CPU. For receive operations, it indicates that the input data register contains the next byte to be read by the DMA controller or CPU.

IRQ — INTERRUPT REQUEST

Output/Active high. The L5380/53C80 asserts this signal to indicate to the microprocessor that one of the several interrupt conditions have been met. These include SCSI bus fault conditions as well as other events requiring microprocessor intervention. Most interrupt types are individually maskable.

$\overline{IOR}$ — I/O READ

Input/Active low. $\overline{IOR}$ is used in conjunction with $\overline{CS}$ and A2–0 to execute a memory mapped read of a L5380/53C80 internal register. It is also used in conjunction with $\overline{DACK}$ to execute a DMA read of the SCSI Input Data Register.

READY — READY

Output/Active high. Ready is used rather than DRQ as an alternate method for controlling DMA data transfer. This DMA type is termed blockmode DMA and must be specifically enabled by the CPU. In block-

mode DMA, data is throttled by treating the L5380/53C80 as wait state memory. I/O (DMA) cycles are initiated at the maximum rate sustainable by the DMA controller/memory subsystem, but all cycles are extended (wait-states inserted) until READY is asserted by the L5380/53C80. This is generally the fastest DMA method since memory subsystem addressing can be overlapped with SCSI operations (flyby mode).

$\overline{DACK}$ — DMA ACKNOWLEDGE

Input/Active low. $\overline{DACK}$ is used in conjunction with $\overline{IOR}$ or $\overline{IOW}$ to enable reading or writing of the SCSI Input and Output Data Registers when in DMA mode. $\overline{DACK}$ resets DRQ and must not occur simultaneously with $\overline{CS}$.

$\overline{EOP}$ — END OF PROCESS

Input/Active low. This input is used to indicate to the L5380/53C80 that a DMA transfer is to be concluded. The L5380/53C80 can automatically generate an interrupt in response to receiving $\overline{EOP}$ from the DMA controller.

$\overline{RESET}$ — CPU BUS RESET

Input/Active low. This input clears all internal registers and state machines. It does not result in assertion of the $\overline{RST}$ signal on the SCSI bus and therefore affects only the local L5380/53C80 and not other devices on the bus.

$\overline{IOW}$ — I/O WRITE

Input/Active low. $\overline{IOW}$ is used in conjunction with $\overline{CS}$ and A_{2-0} to execute a memory mapped write of a L5380/53C80 internal register. It is also used in conjunction with $\overline{DACK}$ to execute a DMA write of the SCSI Output Data Register.

A_{2-0} — ADDRESS 2-0

Inputs/Active high. These signals, in conjunction with $\overline{CS}$, $\overline{IOR}$, and $\overline{IOW}$, address the L5380/53C80 internal registers for CPU read/write operations.

D_{7-0} — DATA 7–0

Bidirectional/Active high. These signals are the microprocessor data bus. D_7 is the most significant bit.

L5380/53C80 INTERNAL REGISTERS

Overview

The L5380/53C80 contains registers that are directly addressed by the microprocessor. These registers allow for monitoring of SCSI bus activity, controlling the operation of the L5380/53C80, and determining the cause of interrupts. In many cases, a read-only and a write-only register are mapped to the same address. Some addresses are dummy registers which are used to implement a control operation but do not correspond to a physical register. The state of the CPU data bus when writing or reading these dummy registers is 'don't care'. Tables 1 and 3 show the address and name of each register as well as bit definitions.

Register Descriptions

A. Write Operations

The following paragraphs give detailed descriptions of the function of each bit in the L5380/53C80 internal registers for write operations as shown in Table 1.

WRITE ADDRESS 0
Output Data Register

The Output Data Register is a write-only register used for sending information to the SCSI data bus. During arbitration, the arbitrating SCSI device asserts its ID via this register. The device which wins arbitration also asserts the "OR" of its ID and the ID of the target/initiator to be selected/reselected. In programmed I/O mode this register is written using $\overline{CS}$ and $\overline{IOW}$ with $A_{2-0} = 000$. In DMA mode, it is written when $\overline{IOW}$ and $\overline{DACK}$ are simultaneously active, irrespective of the state of the address lines. Note that a "1" written to the Output Data Register becomes a low state when asserted on the active-low SCSI bus.

WRITE ADDRESS 1
Initiator Command Register

The Initiator Command Register is a read/write register which allows CPU control of the SCSI signals asserted by the initiator. Some bits in this register are not readable, and these positions are mapped to status bits useful in monitoring the progress of arbitration. These, along with the initiation of system-wide reset and test functions, may also be of use to the target.

R1 Bit 7 — Assert $\overline{RST}$

When this bit is set, the L5380/53C80 asserts the $\overline{RST}$ line on the SCSI bus, initializing all devices on the bus to the reset condition. All logic and internal registers of the L5380/53C80 are reset, except for the Assert RST bit itself, the Testmode bit (R1 bit 6) and the IRQ (interrupt request) latch. The IRQ pin becomes active indicating a SCSI bus reset interrupt. This interrupt is not maskable.

R1 Bit 6 — Testmode

When this bit is set, the L5380/53C80 places all outputs, including both SCSI and CPU signals, in a high impedance state. This effectively removes the device from the system as an aid to system diagnostics. Note that internal registers may still be written to while in Testmode. The L5380/53C80 returns to normal operation when Testmode is reset. The Testmode bit is reset by either writing a "0" to R1 bit 6

or via the $\overline{\text{RESET}}$ (CPU reset) pin. Testmode is not affected by the $\overline{\text{RST}}$ (SCSI bus reset) signal, or by the Assert $\overline{\text{RST}}$ bit in the Initiator Command Register (R1 bit 7).

R1 Bit 5 — Not Used

R1 Bit 4 — Assert $\overline{\text{ACK}}$

When this bit is set, $\overline{\text{ACK}}$ is asserted on the SCSI bus. Resetting this bit deasserts $\overline{\text{ACK}}$. Note that $\overline{\text{ACK}}$ will be asserted only if the Targetmode bit (R2 bit 6) is reset, indicating that the L5380/53C80 is acting as an initiator.

R1 Bit 3 — Assert $\overline{\text{BSY}}$

When this bit is set, $\overline{\text{BSY}}$ is asserted on the SCSI bus. Resetting this bit deasserts $\overline{\text{BSY}}$. $\overline{\text{BSY}}$ is asserted to indicate that the device has been selected or reselected, and deasserting $\overline{\text{BSY}}$ causes a bus free condition.

R1 Bit 2 — Assert $\overline{\text{SEL}}$

When this bit is set, $\overline{\text{SEL}}$ is asserted on the SCSI bus. Resetting this bit deasserts $\overline{\text{SEL}}$. $\overline{\text{SEL}}$ is normally asserted after a successful arbitration.

R1 Bit 1 — Assert $\overline{\text{ATN}}$

When this bit is set, $\overline{\text{ATN}}$ is asserted on the SCSI bus. Resetting this bit deasserts $\overline{\text{ATN}}$. $\overline{\text{ATN}}$ is asserted by the initiator to request message out phase. Note that $\overline{\text{ATN}}$ will be asserted only if the Targetmode bit (R2 bit 6) is reset, indicating that the L5380/53C80 is acting as an initiator.

R1 Bit 0 — Assert Data Bus

When this bit is set, the open drain SCSI data bus and parity drivers are enabled and the contents of the Output Data Register are driven onto the SCSI data lines. In addition to the Assert Data Bus bit, enabling of the SCSI bus drivers requires one of the following two sets of conditions:

When the L5380/53C80 is operating as an initiator, the Targetmode bit (R2 bit 6) must be reset, the $\overline{\text{I}}$/O pin must be negated (initiator to target transfer) and no phase mismatch condition can exist. A phase mismatch occurs when the $\overline{\text{MSG}}$, $\overline{\text{C}}$/D, and $\overline{\text{I}}$/O bits of the Target Command Register (R3) do not match the corresponding SCSI control lines.

When the L5380/L53C80 is operating as a target, the Targetmode bit will be set, and in this case Assert Data Bus will enable the outputs unconditionally.

The Assert Data Bus bit need not be set for arbitration to occur; when the Arbitrate bit (R2 bit 0) is set, and a bus free condition is detected, the data bus will be enabled for arbitration regardless of the state of the Assert Data Bus bit.

Finally, note that the Testmode bit (R1 bit 6) overrides all other controls, including Assert Data Bus and Arbitrate, and disables all outputs.

WRITE ADDRESS 2
Mode Register

The Mode register is a read/write register which provides control over several aspects of L5380/53C80 operation. Programmed I/O or two different types of DMA transfer may be selected, initiator or target device operation is accommodated, and parity checking and interrupts may be enabled via this register. The function of each individual bit is described as follows:

R2 Bit 7 — Blockmode

This bit must be used in conjunction with DMA Mode (R2 bit 1). It is used to select the type of handshake desired between the L5380/53C80 and the external DMA controller. See "L5380/53C80 Data Transfers" for a complete discussion of the transfer types supported.

R2 Bit 6 — Targetmode

When this bit is set, the L5380/53C80 will operate as a SCSI target device. This enables the SCSI signals $\overline{\text{I}}$/O, $\overline{\text{C}}$/D, $\overline{\text{MSG}}$, and $\overline{\text{REQ}}$ to be asserted. When Targetmode is reset, the device will operate as an initiator. This enables the SCSI signals $\overline{\text{ATN}}$ and $\overline{\text{ACK}}$ to be asserted. Targetmode also affects state machine operation for DMA transfers and the conditions necessary for enabling the SCSI Data bus drivers. (See Assert Databus, R1 bit 0).

R2 Bit 5 — Enable Parity Check

When this bit is set, information received on the SCSI data bus is checked for odd parity. The Parity Error latch will be set whenever data is received under DMA control or the Current SCSI Data Register (Read Register 0) is read by the CPU. The state of the Parity Error latch can be determined by reading R5 bit 5, and it can be reset by a read to Address 7. Note that ENABLE PARITY CHECK must be set if parity error interrupts are to be generated. This interrupt can be separately masked by the Enable Parity Interrupt bit (R2 bit 4) while retaining the state of the Parity Error latch for later examination by the CPU.

R2 Bit 4 — Enable Parity Interrupt

When this bit is set, the L5380/53C80 will set the interrupt request latch, and assert IRQ (interrupt request) if it detects a parity error. Enable Parity Check (R2 bit 5) must also be set if parity error interrupts are desired.

R2 Bit 3 — Enable End Of DMA Interrupt

When this bit is set, the L5380/53C80 will set the interrupt request latch, and assert IRQ (interrupt request) if it detects a valid $\overline{\text{EOP}}$ (End of Process) signal. $\overline{\text{EOP}}$ is normally generated by a DMA controller to indicate the end of a DMA transfer. $\overline{\text{EOP}}$ is valid only when coincident with $\overline{\text{IOR}}$ or $\overline{\text{IOW}}$ and $\overline{\text{DACK}}$.

R2 Bit 2 — Monitor Busy

When this bit is set, the L5380/53C80 continuously monitors the state of the $\overline{BSY}$ signal. Absence of $\overline{BSY}$ for a period longer than 400 ns (but less than 1200 ns) will cause the L5380/53C80 to set the BSYERR and IRQ (interrupt request) latches. In addition, the six least significant bits of the Initiator Command Register are reset, and all SCSI data and control outputs are disabled until the BSYERR latch is reset. This effectively disconnects the L5380/53C80 from the SCSI bus in response to an unexpected disconnect by another device. It also allows the CPU to be interrupted when the SCSI bus becomes free in systems where arbitration is not used and an $\overline{EOP}$ signal is not available.

R2 Bit 1 — DMA Mode

When this bit is set, the L5380/53C80's internal state machines automatically control the SCSI signals $\overline{REQ}$ and $\overline{ACK}$ (as appropriate for initiator or target operation) and the CPU signals DRQ and READY. DMA Mode must be set prior to starting a DMA transfer in either direction. The DMA Mode bit is reset whenever a bus free condition is detected ($\overline{BSY}$ is not active). This aborts DMA operations when a loss of $\overline{BSY}$ occurs, regardless of the state of the Monitor Busy bit (R2 bit 2.) The DMA Mode bit is not reset when $\overline{EOP}$ is received, but must be specifically reset by the CPU. $\overline{EOP}$ does, however, inhibit additional DMA cycles from occurring.

R2 Bit 0 — Arbitrate

This bit is set to indicate a desire to arbitrate for use of the SCSI bus. Before setting the Arbitrate bit, the SCSI Output Data Register (Write Register 0) must be written with the SCSI ID assigned to the arbitrating SCSI device. The bit position of register R0 which is set represents the priority number of the SCSI device, with bit 7 the highest priority. See the section on "Arbitration" for a full discussion of the L5380/53C80 arbitration procedure.

TABLE 1. WRITE REGISTERS

Address 0 — Output Data Register

7	6	5	4	3	2	1	0
$\overline{SDB7}$	$\overline{SDB6}$	$\overline{SDB5}$	$\overline{SDB4}$	$\overline{SDB3}$	$\overline{SDB2}$	$\overline{SDB1}$	$\overline{SDB0}$

Address 1 — Initiator Command Register

7	6	5	4	3	2	1	0
ASSERT $\overline{RST}$	TEST MODE		ASSERT $\overline{ACK}$	ASSERT $\overline{BSY}$	ASSERT $\overline{SEL}$	ASSERT $\overline{ATN}$	ASSERT DATA BUS

Address 2 — Mode Register

7	6	5	4	3	2	1	0
BLOCK MODE	TARGET MODE	ENABLE PARITY CHECK	ENABLE PARITY INT'RPT	ENABLE EODMA INT'RPT	MONI-TOR BUSY	DMA MODE	ARBI-TRATE

Address 3 — Target Command Register

7	6	5	4	3	2	1	0
LAST BYTE SENT				ASSERT $\overline{REQ}$	ASSERT $\overline{MSG}$	ASSERT $\overline{C}$/D	ASSERT $\overline{I}$/O

Address 4 — ID Select Register

7	6	5	4	3	2	1	0
$\overline{SDB7}$	$\overline{SDB6}$	$\overline{SDB5}$	$\overline{SDB4}$	$\overline{SDB3}$	$\overline{SDB2}$	$\overline{SDB1}$	$\overline{SDB0}$

Address 5 — Start DMA Send

7	6	5	4	3	2	1	0

Address 6 — Start DMA Target Receive

7	6	5	4	3	2	1	0

Address 7 — Start DMA Initiator Receive

7	6	5	4	3	2	1	0

WRITE ADDRESS 3
Target Command Register

The Target Command Register is a read/write register which allows CPU control of the SCSI signals asserted by the target. In addition, this register contains a read-only status flag useful in unambiguously determining when the last byte of a DMA transfer has actually been sent over the SCSI bus.

When operating as an initiator with DMA mode set, the Assert $\overline{MSG}$, Assert $\overline{C}/D$, and Assert $\overline{I}/O$ bits are used as a template to compare against the corresponding SCSI control signals provided by the target. A phase mismatch interrupt will be generated on the falling edge of the $\overline{REQ}$ input if the template does not match the state of the signals. Therefore the CPU should initialize these bits to the phase of the expected data transfer. An interrupt, then, will signal an intent by the target to change to a new phase. The SCSI information transfer phases and their associated direction of data transfer are given in Table 2.

R3 Bits 7-4 — Not Used

R3 Bit 3 — Assert $\overline{REQ}$

When this bit is set, $\overline{REQ}$ is asserted on the SCSI bus. Resetting this bit deasserts $\overline{REQ}$. Note that $\overline{REQ}$ will be asserted only if the Targetmode bit (R2 bit 6) is set, indicating that the L5380/53C80 is acting as a target.

R3 Bit 2 — Assert $\overline{MSG}$

When this bit is set, $\overline{MSG}$ is asserted on the SCSI bus. Resetting this bit deasserts $\overline{MSG}$. Note that $\overline{MSG}$ will be asserted only if the Targetmode bit (R2 bit 6) is set, indicating that the L5380/53C80 is acting as a target. When operating as an initiator, this bit is compared against the $\overline{MSG}$ input, and an interrupt is generated if they differ at the falling edge of $\overline{REQ}$.

R3 Bit 1 — Assert $\overline{C}/D$

When this bit is set, $\overline{C}/D$ is asserted on the SCSI bus. Resetting this bit deasserts $\overline{C}/D$. Note that $\overline{C}/D$ will be asserted only if the Targetmode bit (R2 bit 6) is set, indicating that the L5380/53C80 is acting as a target. When operating as an initiator, this bit is compared against the $\overline{C}/D$ input, and an interrupt is generated if they differ at the falling edge of $\overline{REQ}$.

R3 Bit 0 — Assert $\overline{I}/O$

When this bit is set, $\overline{I}/O$ is asserted on the SCSI bus. Resetting this bit deasserts $\overline{I}/O$. Note that $\overline{I}/O$ will be asserted only if the Targetmode bit (R2 bit 6) is set, indicating that the L5380/53C80 is acting as a target. When operating as an initiator, this bit is compared against the $\overline{I}/O$ input, and an interrupt is generated if they differ at the falling edge of $\overline{REQ}$.

WRITE ADDRESS 4
ID Select Register

The ID Select Register is a write-only register which is used to monitor selection or reselection attempts to the L5380/53C80. In arbitrating systems, an ID number is assigned to each SCSI device by setting a single bit position of the ID Select Register. Each SCSI data pin is inverted and compared with the corresponding bit in the ID Select Register. If any matches are found while a bus free condition exists and $\overline{SEL}$ is active, the L5380/53C80 will generate an interrupt to indicate a selection or reselection. During selection or reselection, parity checking may be enabled by setting the Enable Parity Check bit (R2 bit 5). This interrupt may be masked by resetting all bits in this register.

WRITE ADDRESS 5
Start DMA Send

This is a dummy register. Writes to this location are detected and cause the L5380/53C80 internal state machine to execute a DMA send operation. This location is used for either initiator or target DMA send. The DMAMODE bit (R2 bit 1) must be set prior to writing this location.

WRITE ADDRESS 6
Start DMA Target Receive

This is a dummy register. Writes to this location are detected and cause the L5380/53C80 internal state machine to execute a target DMA receive operation. The DMAMODE bit (R2 bit 1) and the Targetmode bit (R2 bit 6) must be set prior to writing this location.

WRITE ADDRESS 7
Start DMA Initiator Receive

This is a dummy register. Writes to this location are detected and cause the L5380/53C80 internal state machine to execute an initiator DMA

TABLE 2. SCSI INFORMATION TRANSFER PHASES

$\overline{MSG}$	$\overline{C}/D$	$\overline{I}/O$	Phase	Direction		
0	0	0	Message In	Target	→	Initiator
0	0	1	Message Out	Initiator	→	Target
0	1	0	Unused			
0	1	1	Unused			
1	0	0	Status In	Target	→	Initiator
1	0	1	Command	Initiator	→	Target
1	1	0	Data In	Target	→	Initiator
1	1	1	Data Out	Initiator	→	Target

receive operation. The DMAMODE bit (R2 bit 1) must be set and the Targetmode bit (R2 bit 6) must be reset prior to writing this location.

B. READ OPERATIONS

The following paragraphs give detailed descriptions of the function of each bit in the L5380/53C80 internal registers for read operations as shown in Table 3.

READ ADDRESS 0
Current SCSI Data Bus

The Current SCSI Data Bus Register allows the microprocessor to monitor the SCSI data bus at any time, by asserting $\overline{CS}$ and $\overline{IOR}$ with address lines A_{2-0} = 000. The SCSI data lines are not actually registered, but gated directly onto the CPU bus whenever Address 000 is read by the CPU. Therefore, reads of this location should only be done when the SCSI data lines are guaranteed to be stable by the SCSI protocol. For systems which implement SCSI bus arbitration, this location is read to determine whether devices having higher priorities are also arbitrating. Programmed I/O data transfer uses this location for reading data transferred on the SCSI data bus. With parity checking enabled, SCSI data bus parity checking is done at the beginning of the read cycle for fast error detection. Note that the SCSI data bus is inverted to become active high when presented to the CPU.

READ ADDRESS 1
Initiator Command Register

Reading bit 7 or bits 4–0 of the Initiator Command Register simply reflects the status of the corresponding bit in the register. Bits 6 and 5 are mapped to other signals as discussed below:

R1 Bit 6 — Arbitration In Progress

For this bit to be active, the Arbitrate bit (R2 bit 0) must be set. When ARBITRATION IN PROGRESS is set, it indicates that the L5380/53C80 has detected a bus free condition and is currently arbitrating for control of the bus. See the section on "Arbitration" for a complete discussion of the L5380/53C80 arbitration mechanism. Resetting the Arbitrate bit will reset ARBITRATION IN PROGRESS.

R1 Bit 5 — Lost Arbitration

For this bit to be active, the Arbitrate bit (R2 bit 0) must be set. When LOST ARBITRATION is set, it indicates that the L5380/53C80 has arbitrated for the SCSI bus (see R1 bit 6 above) and has detected the assertion of $\overline{SEL}$ by another (higher priority) device. The L5380/53C80 responds to loss of arbitration by immediately discontinuing the arbitration attempt. Resetting the Arbitrate bit will reset LOST ARBITRATION.

READ ADDRESS 2
Mode Register

Reading the Mode Register simply reflects the status of the bits in that register.

READ ADDRESS 3
Target Command Register

Reading the Target Command Register simply reflects the status of the bits in that register, except for bit 7, LAST BYTE SENT.

R3 bit 7 — Last Byte Sent

This read only bit indicates that the last byte of data loaded into the L5380/53C80 during a DMA send operation has actually been transferred over the SCSI bus. Note that the end of process flag and the corresponding interrupt occur when this byte is loaded into the L5380/53C80, but do not reflect whether it has actually been sent. This bit is not present in the NCR5380, but is present in the NCR53C80. Last Byte Sent is reset when the DMAMODE bit (R2 bit 1) is reset.

READ ADDRESS 4
Current SCSI Control Register

The Current SCSI Control Register provides a means for the CPU to directly monitor the state of the SCSI bus control signals. The SCSI control lines are not actually registered, but gated directly onto the CPU bus whenever Address 100 is read by the CPU. The value of each bit position represents the complement of the corresponding (low true) SCSI Signal Pin.

READ ADDRESS 5
DMA Status Register

The DMA Status Register provides a means for the CPU to determine the status of a DMA transfer and to determine the cause of an interrupt. It also makes available the final two SCSI bus signals which are not included in the Current SCSI Control Register. The function of each individual bit is defined as follows:

R5 Bit 7 — End of DMA

When this bit is set, it indicates that a valid $\overline{EOP}$ has been received during a DMA transfer. A valid $\overline{EOP}$ occurs when $\overline{EOP}$, $\overline{DACK}$, and either $\overline{IOR}$ or $\overline{IOW}$ are simultaneously active for the minimum specified time. End of DMA is reset when the DMAMODE bit (R2 bit 1) is reset.

Note that for DMA send operations, an END OF DMA status indicates only that the last byte of the transfer is loaded into the Output Data Register of the sending device, not that it has actually been transferred over the SCSI bus. For this reason, the L5380/53C80 provides an additional status bit; Last Byte Sent (R3 bit 7) which indicates that this final byte has been transferred to the receiving end. This bit is not present in the NCR5380.

Also, note that the DMAMODE bit is reset automatically whenever a loss of busy condition is detected, which in turn resets END OF DMA. Therefore

the DMA Status Register should be read prior to resetting the Assert $\overline{BSY}$ bit (R1 bit 3) at the conclusion of a DMA transfer.

R5 Bit 6 — DMA Request

This bit reflects the state of the DRQ (DMA Request) signal. In programmed I/O, this bit can be polled by the CPU to determine whether there is a pending request for byte transfer. For DMA send operations, DMA REQUEST is reset when $\overline{DACK}$ and $\overline{IOW}$ are simultaneously asserted. For DMA receive operations, simultaneous $\overline{DACK}$ and $\overline{IOR}$ will reset DMA REQUEST. DMA REQUEST is reset unconditionally when the DMAMODE bit (R2 bit 1) is reset.

R5 Bit 5 — Parity Error

This bit can only be set if Enable Parity Check (R2 bit 5) is set. When enabled, the Parity Error bit is set if incoming SCSI data in either initiator or target mode, or during selection phase, does not correctly reflect odd parity. PARITY ERROR can be reset by a read to the Reset Error/Interrupt Register (Register 7).

R5 Bit 4 — Interrupt Request

This bit reflects the state of the IRQ signal. The L5380/53C80 asserts IRQ to generate an interrupt to the CPU. See the section on "Interrupts" for further information on the possible sources of interrupts in the L5380/53C80. INTERRUPT REQUEST can be reset by a read to the Reset Error/Interrupt Register (Register 7).

R5 Bit 3 — Phase Match

When this bit is set, it indicates that the $\overline{MSG}$, $\overline{C}$/D, and $\overline{I}$/O lines match the state of the Assert $\overline{MSG}$, Assert $\overline{C}$/D, and Assert $\overline{I}$/O bits in the Target Command Register. PHASEMATCH is not actually registered, but represents a continuous comparison of these three phase bits to the corresponding internal register locations. This bit is intended for use by the

TABLE 3. READ REGISTERS

Address 0 — Current SCSI Data Bus

7	6	5	4	3	2	1	0
$\overline{SDB7}$	$\overline{SDB6}$	$\overline{SDB5}$	$\overline{SDB4}$	$\overline{SDB3}$	$\overline{SDB2}$	$\overline{SDB1}$	$\overline{SDB0}$

Address 1 — Initiator Command Register

7	6	5	4	3	2	1	0
ASSERT $\overline{RST}$	ARB. IN PRO-GRESS	LOST ARB.	ASSERT $\overline{ACK}$	ASSERT $\overline{BSY}$	ASSERT $\overline{SEL}$	ASSERT $\overline{ATN}$	ASSERT DATA BUS

Address 2 — Mode Register

7	6	5	4	3	2	1	0
BLOCK MODE	TARGET MODE	ENABLE PARITY CHECK	ENABLE PARITY INT'RPT	ENABLE EODMA INT'RPT	MONI-TOR BUSY	DMA MODE	ARBI-TRATE

Address 3 — Target Command Register

7	6	5	4	3	2	1	0
LAST BYTE SENT				ASSERT $\overline{REQ}$	ASSERT $\overline{MSG}$	ASSERT $\overline{C}$/D	ASSERT $\overline{I}$/O

Address 4 — Current SCSI Control Register

7	6	5	4	3	2	1	0
$\overline{RST}$	$\overline{BSY}$	$\overline{REQ}$	$\overline{MSG}$	$\overline{C}$/D	$\overline{I}$/O	$\overline{SEL}$	$\overline{PARITY}$

Address 5 — DMA Status Register

7	6	5	4	3	2	1	0
END OF DMA	DMA REQ.	PARITY ERROR	INTER-RUPT REQ.	PHASE MATCH	BUSY ERROR	$\overline{ATN}$	$\overline{ACK}$

Address 6 — Input Data Register

7	6	5	4	3	2	1	0
$\overline{SDB7}$	$\overline{SDB6}$	$\overline{SDB5}$	$\overline{SDB4}$	$\overline{SDB3}$	$\overline{SDB2}$	$\overline{SDB1}$	$\overline{SDB0}$

Address 7 — Reset Error/Interrupt Register

7	6	5	4	3	2	1	0

initiator to detect that the target device has changed to a different information transfer phase. When the L5380/53C80 detects a phase mismatch, PHASEMATCH is reset, and information transfer to or from the SCSI bus is inhibited.

R5 Bit 2 — Busy Error

This bit can only be set if the Monitor Busy bit (R2 bit 2) is set. When set, Busy Error indicates that the BSY pin has been false for a period at least equal to a bus settle delay (400 ns). When the Busy Error condition is detected, all SCSI signal pins are disabled, and the DMAMODE bit (R2 bit 1) and bits 5-0 of the Initiator Command Register are reset. Busy Error can be reset by a read to the Reset Error/Interrupt Register (Register 7).

R5 Bits 1, 0 — $\overline{ATN}$, $\overline{ACK}$

Like the Current SCSI Control Register, these bits provide a means for the CPU to directly monitor the state of the SCSI bus control signals. The SCSI control lines are not actually registered, but gated directly onto the CPU bus whenever Address 5 is read by the CPU. The value of each bit position represents the complement of the corresponding (low true) SCSI Signal Pin.

READ ADDRESS 6
Input Data Register

This register acts as a temporary holding register for information received from the SCSI data bus during DMA transfers (DMAMODE bit, R2 bit 1 is set). In the initiator mode, the L5380/53C80 latches the SCSI data when $\overline{REQ}$ goes active. In the target mode, data is latched when $\overline{ACK}$ goes active. The contents of this register represent the negation of the low-true SCSI data. The contents of the SCSI Input Data Register are gated onto the CPU data bus when $\overline{DACK}$ and $\overline{IOR}$ are simultaneously true, or by a CPU read of location 6. Note that $\overline{DACK}$ and $\overline{CS}$ must never be active simultaneously in order to prevent conflicting read operations. Parity may optionally be checked on the data as it is loaded into this register.

READ ADDRESS 7
Reset Error/Interrupt Register

This is a dummy register. Reads to this location are detected and used to reset the Interrupt Request Latch (IRQ signal) and the PARITY ERROR, INTERRUPT REQUEST, and BUSY ERROR latches (visible as bits 5, 4, and 2 of Register 5).

INTERRUPTS

The L5380/53C80 generates interrupts to the CPU by setting the Interrupt Request Latch, which directly drives the IRQ (Interrupt Request) line. The IRQ output will reflect the state of the Interrupt Request Latch under all conditions except when Testmode (R1 bit 6) is active, when it is in a high impedance state. The Interrupt Request Latch may be reset by reading Address 7, the Reset Error/Interrupt Register. A read of this location also resets several error condition latches as discussed in the section on "Internal Registers".

Interrupts may be caused by any of six conditions, most of which may be masked by resetting enable bits in the appropriate registers. The following sections describe each interrupt type, its cause, and how it may be reset. Upon receiving an interrupt, the CPU may read the Current SCSI Control Register (R4) and the DMA Status Register (R5) to determine the cause of the interrupt. While the following discussions indicate the expected values of these registers following an interrupt, it is recommended that bits in these registers which are not germane to determining the cause of an interrupt be masked off in firmware prior to implementing a comparison. A typical operational sequence for an interrupt service routine is given at the end of this section.

SCSI Bus Reset Interrupt

A SCSI Bus Reset Interrupt occurs when the SCSI $\overline{RST}$ signal becomes active. This may be due to another SCSI device driving the $\overline{RST}$ line, or because the Assert $\overline{RST}$ bit (R1 bit 7) has been set, causing the L5380/53C80 to drive the SCSI $\overline{RST}$ line. The value of the SCSI $\overline{RST}$ line is visible as R4 bit 7; however, this line is not latched and therefore may have changed state by the time the CPU responds to the interrupt and polls this location. For this reason, a SCSI Bus Reset Interrupt should be assumed if no other interrupt condition is active when reading Registers 4 and 5.

The SCSI Bus Reset Interrupt is nonmaskable. The expected read values for the Current SCSI Control Register and the DMA Status Register upon encountering this interrupt are given in Table 4.

Selection/Reselection Interrupt

A Selection/Reselection Interrupt occurs when the SCSI $\overline{SEL}$ signal becomes active, the SCSI bus matches the bit set in the ID Select Register, and $\overline{BSY}$ has been false for at least a bus settle delay. When the $\overline{I}$/O pin is asserted, the interrupt should be interpreted as a reselection. The Selection/Reselection Interrupt may be masked by resetting all bits in the ID Select Register. The expected read values for the Current SCSI Control Register and the DMA Status Register upon encountering this interrupt are given in Table 4.

Loss of Busy Interrupt

A Loss of Busy Interrupt occurs when the SCSI $\overline{BSY}$ signal has been inactive for at least a bus settle delay (400 ns). The Loss of Busy Interrupt may be masked by resetting the Monitor Busy bit (R2 bit 2). Resetting Monitor Busy also prevents the Busy Error latch (Read R5 bit 2) from being set. The expected read values for the Current

SCSI Control Register and the DMA Status Register upon encountering this interrupt are given in Table 4.

Phase Mismatch Interrupt

A Phase Mismatch Interrupt occurs when the DMAMODE bit (R2 bit 1) is set, $\overline{REQ}$ is active on the SCSI bus, and the SCSI phase signals $\overline{MSG}$, $\overline{C}$/D, and $\overline{I}$/O do not match the corresponding bits in the Target Command Register. This interrupt is intended for use by the initiator to detect a change of phase by the target during a DMA transfer. When operating as a target, the SCSI phase lines will normally be asserted via the Target Command Register, so no phase mismatch will be generated unless another SCSI device is erroneously driving the phase lines to an unintended state.

The result of the continuous comparison of the SCSI phase lines to the Target Command Register contents is visible as the Phase Match bit (Read R5 bit 3). This flag operates irrespective of the state of DMAMODE and $\overline{REQ}$. As long as a phase mismatch condition persists, the L5380/53C80 is prevented from recognizing active $\overline{REQ}$ inputs, and SCSI output data drivers are disabled.

The Phase Mismatch Interrupt is nonmaskable, however it will only occur when operating in DMAMODE. The expected read values for the Current SCSI Control Register and the DMA Status Register upon encountering this interrupt are given in Table 4.

Parity Error Interrupt

A Parity Error Interrupt occurs when incorrect parity is detected during a read of the SCSI bus. Parity checking occurs under the following conditions: Parity is checked during a programmed I/O read of the Current SCSI Data Register (Read R0), when $\overline{CS}$ and $\overline{IOR}$ are active and the A_{2-0} lines are 000. Parity is also checked during DMA read operations (DMAMODE bit, R2 bit 1 is set) when $\overline{ACK}$ is active for target receive, or $\overline{REQ}$ is active for initiator receive.

The Parity Error latch is set when parity error checking is enabled and one of the above parity error conditions is encountered. This latch is

TABLE 4. INTERRUPT READ VALUES

Read Address 4 — Current SCSI Control Register

7	6	5	4	3	2	1	0
$\overline{RST}$	$\overline{BSY}$	$\overline{REQ}$	$\overline{MSG}$	$\overline{C}$/D	$\overline{I}$/O	$\overline{SEL}$	$\overline{PARITY}$
SCSI Bus Reset Interrupt							
X	0	0	0	0	0	0	0
Selection/Reselection Interrupt							
0	0	0	X	X	1=RESEL	1	X
Loss of Busy Interrupt							
0	0	0	0	0	0	0	0
Phase Mismatch Interrupt							
0	1	1	X	X	X	0	X
Parity Error Interrupt							
0	X	X	X	X	X	X	X
End of DMA Interrupt							
0	1	X	X	X	X	0	X

Read Address 5 — DMA Status Register

7	6	5	4	3	2	1	0
END OF DMA	DMA REQ	PARITY ERROR	INTER-RUPT REQ	PHASE MATCH	BUSY ERROR	$\overline{ATN}$	$\overline{ACK}$
SCSI Bus Reset Interrupt							
0	0	0	1	1	0	0	0
Selection/Reselection Interrupt							
0	0	0	1	X	0	X	0
Loss of Busy Interrupt							
0	0	0	1	X	1	0	0
Phase Mismatch Interrupt							
0	0	0	1	0	X	X	0
Parity Error Interrupt							
X	X	1	1	X	X	X	X
End of DMA Interrupt							
1	0	0	1	X	0	0	X

visible as bit 5 of the DMA Status Register (Read R5). The Parity Error Interrupt may be masked and setting of the Parity Error latch prevented by resetting the Enable Parity Check bit (Write R2 bit 5). The Parity Error latch can be reset by reading the Reset Error/Interrupt Register (Read R7). The expected read values for the Current SCSI Control Register and the DMA Status Register upon encountering this interrupt are given in Table 4.

End of DMA Interrupt

An End of DMA Interrupt occurs when a valid $\overline{EOP}$ (End of Process) signal is detected during a DMA transfer. $\overline{EOP}$ is valid when $\overline{EOP}$, $\overline{DACK}$, and either $\overline{IOR}$ or $\overline{IOW}$ are simultaneously asserted for the minimum specified time. $\overline{EOP}$ inputs not occurring during I/O read or write operations are ignored.

The End of DMA latch is set whenever the DMAMODE bit (R2 bit 1) is set and a valid $\overline{EOP}$ is received. This latch is visible as bit 7 of the DMA Status Register (Read R5). The End of DMA Interrupt may be masked by resetting the Enable EODMA Interrupt bit (Write R2 bit 3). This bit does not affect the End of DMA latch, however. The End of DMA latch can be reset by resetting the DMAMODE bit in the Mode Register. The expected read values for the Current SCSI Control Register and the DMA Status Register upon encountering this interrupt are given in Table 4.

DATA TRANSFERS

The L5380/53C80 supports programmed I/O under CPU control or DMA transfer via a DMA controller when transferring information to and from the SCSI data bus. Programmed I/O can be implemented entirely in firmware or using minimum external logic for accessing the appropriate registers. Under DMA control, the L5380/53C80's DMA interface logic and internal state machines provide the necessary control of the $\overline{REQ}$-$\overline{ACK}$ handshake. Each type of transfer is fully described in the following sections.

Programmed I/O

Two forms of programmed I/O are supported by the L5380/53C80. For normal programmed I/O, the SCSI handshake is accomplished by setting bits in the Initiator or Target Command registers to assert SCSI control lines, and polling the Current SCSI Control and DMA Control registers for the appropriate responses. Since for this method the control is contained in firmware, the cycle times are relatively slow. It is most appropriate for transferring small blocks of data such as SCSI command blocks or messages, where the overhead of setting up a DMA controller could be significant.

Pseudo DMA

An alternate method of programmed I/O allows the state machines of the L5380/53C80 to handle the SCSI handshake, thereby improving performance in systems which do not employ a hardware DMA controller. To implement Pseudo DMA, the DMAMODE bit is set. The CPU polls the DRQ bit in the DMA Control Register to determine when a byte should be written to or read from the

TABLE 5. TYPICAL INTERRUPT SERVICE ROUTINE POLLING SERVICE

Read Address 5 > TEMP	: Read DMA Status Reg to variable TEMP
IF TEMP "AND" HEX (10) = 0 THEN GO TO NEXT DEVICE	: IRQ not active, so L5380/L53C80 was not the source of this interrupt
TEMP "AND" HEX (AC) → TEMP	: Mask off irrevelant bits
IF TEMP > HEX (7F) THEN GO TO EODMA	: End of DMA Interrupt
IF TEMP > HEX (1F) THEN GO TO PARERR	: Parity Error Interrupt
IF TEMP > HEX (03) THEN GO TO BYSERR	: Loss of Busy Interrupt
IF TEMP = HEX (00) THEN GO TO PHASERR	: Phase Mismatch Interrupt
Read Address 4 → TEMP	: Read Current SCSI Control Reg to variable TEMP
TEMP "AND" HEX (06) → TEMP	: Mask off irrevelant bits
IF TEMP = HEX (06) THEN GO TO RESEL	: Reselection Interrupt
IF TEMP = HEX (02) THEN GO TO SEL	: Selection Interrupt
IF TEMP = HEX (00) THEN GO TO RESET	: SCSI Bus Reset Interrupt

L5380/53C80. When reading or writing, external logic must be used to decode the L5380/53C80 location and produce $\overline{DACK}$, since it is used by the internal state machines. Also, $\overline{CS}$ must be suppressed since it may not be asserted simultaneously with $\overline{DACK}$.

Normal DMA Mode

Normal DMA mode is obtained when the DMAMODE bit is set but the Blockmode bit is reset. The DMA process is started by writing to the Start DMA Send, Start DMA Initiator Receive, or Start DMA Target Receive locations as appropriate. Once started, the internal state machines of the L5380/53C80 manage the $\overline{REQ}$ - $\overline{ACK}$ handshake protocol, as well as the DRQ-$\overline{DACK}$ handshake with the DMA controller.

The L5380/53C80 will assert DRQ whenever it is ready to transfer a byte to or from the DMA controller. In response to DRQ, the controller asserts $\overline{DACK}$ and $\overline{IOR}$ to read the byte, or $\overline{DACK}$ and $\overline{IOW}$ to write a byte to the L5380/53C80. For write operations, the byte is latched at the rising edge of the logical AND of $\overline{DACK}$ and $\overline{IOW}$. The transfer can be terminated by asserting $\overline{EOP}$ during a read or write operation, or by resetting the DMAMODE bit.

Block DMA Mode

When the Blockmode bit is set, the DMA handshake is no longer dependent on interlocked DRQ-$\overline{DACK}$ cycles. Instead, the DMA controller may be allowed to free-run, with data flow throttled by inserting "wait-states" in the DMA transfer to or from the L5380/53C80. Wait-states, which are idle clock cycles inserted during the I/O read or write operation, are inserted by the DMA controller until the READY output of the L5380/53C80 goes true, allowing the bus cycle to conclude.

The READY output will be deasserted under the following conditions: For send operations, READY will be false whenever the Output Data Register contains a byte which has not been transferred over the SCSI bus. This allows the DMA controller to access RAM to fetch the next byte, but postpones the end of the CPU bus cycle until the previous byte has been transferred, freeing the Output Data Register to receive it.

For receive operations, READY will be false whenever the Input Data Register is empty. This allows the DMA controller to address the RAM for a write operation, but postpones the end of the CPU bus cycle until the incoming byte is stored in the Input Data Register and is available on the CPU bus.

Note that when blockmode is employed, $\overline{DACK}$ may optionally remain asserted throughout the DMA transfer, since it is not used in an interlocked DMA handshake (Its interlock function is replaced by $\overline{IOR}$ or $\overline{IOW}$). Also, DRQ will be asserted in the normal way when operating in blockmode. To gain the abovementioned performance benefits, it should be used only to initiate the first byte transfer, with READY used to throttle succeeding transfers. This methodology is compatible with DMA controllers such as the Intel 8237 and AMD Am9516/9517.

In summary, blockmode operation offers the potential for improved transfer rates by overlapping the DMA memory access with the SCSI transfer. This is of particular value when used with DMA controllers capable of "flyby" operation, where the data is transferred directly from memory to the peripheral, and does not pass through the DMA controller itself. This transfer rate gain is achieved at the expense of locking up the CPU bus for a time equal to the SCSI transit time of the entire block. This may be strongly preferable in some systems where net disk access time is a crucial performance factor. Also, the time required to arbitrate for the CPU bus on a byte-by-byte basis may well be longer than the cycles wasted waiting for SCSI transfers to take place, especially with fast peripherals which operate from a high speed sector buffer.

Terminating DMA Transfers

DMA transfers, either normal or blockmode, may be terminated in a number of ways. The following sections describe these methods, along with providing information about correct sequencing of various signals to effect a clean exit from a DMA process.

$\overline{EOP}$ Signal

The $\overline{EOP}$ signal is usually generated by a DMA controller to indicate that its transfer counter has decremented to zero. In order to be recognized by the L5380/53C80, it should be asserted simultaneously with the $\overline{DACK}$ and $\overline{IOR}$ or $\overline{IOW}$ signals corresponding to the last byte in the transfer. Note that in the case of send operations, asserting $\overline{EOP}$ indicates to the L5380/53C80 that SCSI transfers should cease after transmission of the byte loaded while $\overline{EOP}$ is asserted. In order to determine when this last byte has actually been sent, the Last Byte Sent flag in the Target Command Register may be examined. This flag is not present in the NCR implementation of the 5380, but is available in the 53C80, a non-pin-compatible variant. The $\overline{EOP}$ input does not reset the DMAMODE bit, but after transmission of the last byte causes the internal state machine to return to an idle condition, so that no further SCSI handshaking will occur until another transmission is explicitly initiated. Note that the NCR version of the 5380, upon receiving an $\overline{EOP}$, will stop asserting DRQ, but will continue to issue $\overline{ACK}$ in response to additional $\overline{REQ}$ inputs,

potentially causing data loss if the target initiates another data transmission without an intervening phase change. The L5380/53C80 prevents this spurious DMA handshake from occurring.

DMA Mode Bit

Resetting the DMAMODE bit in the Mode Register causes a hard reset of the internal DMA state machines, and thus an effective termination of a DMA transfer. Since unlike the $\overline{EOP}$ case the state machine is not allowed to exit gracefully, care must be taken in the timing of DMAMODE reset.

For receive operations, the DMAMODE bit should be reset after the last DRQ is received, but prior to asserting $\overline{DACK}$ to prevent an additional $\overline{REQ}$ or $\overline{ACK}$ from occurring. For normal DMA mode, resetting this bit will cause DRQ to go inactive. However, the last byte received remains in the SCSI Input Data Register and may be read either by the normal $\overline{DACK}$ and $\overline{IOR}$ DMA read or using a CPU read of Address 6. For blockmode DMA, READY will remain asserted when DMAMODE is reset, allowing the DMA controller to retrieve the last byte in the normal fashion. The NCR version of the 5380 fails to keep READY asserted when DMAMODE is reset, potentially causing deadlock on the CPU bus.

Bus Phase Mismatch

When operating in DMAMODE as an initiator, a bus phase mismatch can be used to terminate a data transfer. If the $\overline{C}$/D, $\overline{I}$/O, and $\overline{MSG}$ lines fail to match the corresponding bits in the Target Command Register, it will prevent recognition of $\overline{REQ}$, and will disable the SCSI data and parity output drivers. Also, when $\overline{REQ}$ becomes active, an interrupt will be generated. Because $\overline{REQ}$ is not recognized, the effect is to stop the DMA transfer, although the state machine does not return to idle until either DMAMODE is reset or a valid $\overline{EOP}$ is received.

One caution should be observed when using phase changes to end DMA transfers: While this method does not require the initiator to keep a transfer counter, it depends on the target causing a phase change between any two consecutive information transfer phases. Since this is not required by the protocol, it must be guaranteed by the target software. Otherwise the target may begin a new information transfer without the initiator recognizing the boundary between the two.

ARBITRATION

The L5380/53C80 contains on-chip hardware to assist in arbitrating for the SCSI bus. This arbitration logic cooperates with the host firmware to effect SCSI arbitration, as described in the following paragraphs:

The SCSI arbitration timeline begins with detection of a bus free condition at time t_0. Bus free is defined as $\overline{BSY}$ and $\overline{SEL}$ inactive for at least a bus settle delay (400 ns). Following the bus settle delay, the SCSI device must wait an additional bus free delay of 800 ns, for a total of 1200 ns after t_0, prior to driving any signal. Thus a minimum of 1200 ns must elapse from initial deassertion of $\overline{BSY}$ to the beginning of an arbitration attempt. A final constraint is that arbitration may not begin if more than a bus set delay (1800 ns) has elapsed since $\overline{BSY}$ became active (arbitration began), corresponding to 2200 ns after t_0.

The CPU indicates a desire to arbitrate by setting the Arbitrate bit (R2 bit 0). When Arbitrate is set, the L5380/53C80 will monitor the state of $\overline{BSY}$ and $\overline{SEL}$ to detect a bus free condition. The actual implementation uses an internal delay line to provide a time reference for detection of a bus free condition. This delay is nominally 800 ns during which $\overline{BSY}$ and $\overline{SEL}$ must be inactive. This time represents the center of the window between the Bus Settle Delay (400 ns) and the Bus Free Delay (400 + 800 = 1200 ns). When Bus Free is detected, the L5380/53C80 waits for an additional time of nominally 900 ns (1700 ns nominal since t_0) and asserts $\overline{BSY}$ and the contents of the Output Data Register. This time represents the center of the 1200 ns–2200 ns window between the earliest and latest legal arbitration attempt. Since the actual delays are process and temperature dependent, they will vary in practice, but will always remain well within the specified limits.

Once arbitration has begun ($\overline{BSY}$ and the Output Data Register asserted,) the Arbitration In Progress bit (R1 bit 6) will be set, allowing the CPU to detect the fact that arbitration has begun. The CPU should then wait one arbitration delay (2.2 µs) before reading the bus to determine whether arbitration has been won or lost. The Lost Arbitration bit (R2 bit 7) will be active if the L5380/53C80 has detected $\overline{SEL}$ active on the SCSI bus, indicating that another SCSI device has declared itself the winner of the arbitration. $\overline{SEL}$ active also disables the SCSI output drivers, allowing the winning arbitrator to proceed with its transfer.

BUG FIXES/ENHANCMENTS

The NCR5380 and the Am5380 have some architectural bugs, both published and unpublished. The **LOGIC Devices L5380/53C80** was designed to eliminate these bugs while maintaining pin and architectural compatibility. A list of these errors along with solutions implemented in the L5380/53C80 is itemized below.

1. When executing blockmode DMA send operations, the READY signal is intended to insert memory wait states as a mechanism to throttle data transfer, with the DMA controller in a free-running loop. The NCR/Am5380 erroneously allows the contents of the Output Data Register to be overwritten by subsequent bytes prior to acknowledgment of the

current byte by the SCSI receiver. This causes loss of data when operating in blockmode if the sender's DMA cycle is faster than the receiver's.

2. Assertion of $\overline{EOP}$ during blockmode DMA transfers fails to cause assertion of READY in the NCR/Am5380. This may prevent the CPU from becoming bus master and can result in lockup of the CPU bus in a not-ready state. In block DMA send mode when $\overline{EOP}$ is received, the L5380/53C80 reasserts READY immediately after transmitting the final byte. For receive mode, READY is asserted immediately.

3. When a valid $\overline{EOP}$ is detected, the NCR/Am5380 prevents assertion of additional DRQ's, but continues to respond to SCSI handshakes. This means that additional data transmitted without phase change may be lost. The L5380/53C80, like the NCR/Am5380 remains in DMAMODE after an $\overline{EOP}$. However, the internal state machine returns to an idle condition and does not respond to additional SCSI handshake attempts until another data transfer is explicitly initiated.

4. When operating as an initiator in DMAMODE, the NCR/Am5380 leaves $\overline{ACK}$ asserted after receipt of a valid $\overline{EOP}$, requiring the CPU to deassert it. When a valid $\overline{EOP}$ is detected, the L5380/53C80 deasserts $\overline{ACK}$ properly.

5. If the NCR/Am5380 is not terminated on the SCSI side, the floating $\overline{RST}$ pin will cause spurious interrupts. The L5380/53C80 contains internal high value pullups to set unterminated SCSI pins to the inactive state.

6. During DMA send operations, when a valid $\overline{EOP}$ signal is received by the NCR/Am5380, no convenient indication exists to indicate that the last byte of data (loaded simultaneously with $\overline{EOP}$) has in fact been successfully transmitted. The L5380/53C80 provides Last Byte status bit mapped to bit 7 of the Target Command Register. This bit will be set after a valid $\overline{EOP}$ has occurred, and the final byte has been transmitted successfully.

7. During the reselection phase, the NCR/AM5380 may reset the reselection interrupt if the contents of the Target Command Register do not match the current SCSI bus phase. The L5380/53C80 does not spuriously reset this interrupt.

8. In the NCR/Am5380, the phase mismatch interrupt is captured in an edge triggered fashion on the active edge of $\overline{REQ}$. During reselection, this interrupt might not be generated even though a phase change has occurred. The reason for this is as follows:

- The initiator DMAMODE bit must be set in order to receive a phase-match interrupt.
- However, the DMAMODE bit cannot be set unless $\overline{BSY}$ is active.
- $\overline{BSY}$ will be driven active by the target only after the relesection has occurred.
- Once $\overline{BSY}$ has been asserted by the target, it may then assert $\overline{REQ}$ before the initiator has set the DMAMODE bit, and the initiator will then fail to generate an interrupt.

The L5380/53C80 interrupt latch will be set if a phase mismatch condition exists when the later of $\overline{REQ}$ or DMAMODE become active. In this way, the mismatch will always be detected, even if the target asserts $\overline{REQ}$ before the initiator sets DMAMODE.

MAXIMUM RATINGS *Above which useful life may be impaired*

Storage temperature ..... –65°C to +150°C
VCC supply voltage with respect to ground ..... –0.5 V to +7.0 V
Output voltage ..... 0.0 V to **V**CC
Input voltage ..... 0.0 V to +5.5 V
IOL Low Level Output Current (SCSI Bus) ..... 48 mA
IOL Low Level Output Current (other pins) ..... 8 mA
IOH High Level Output Current (other pins) ..... –4 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

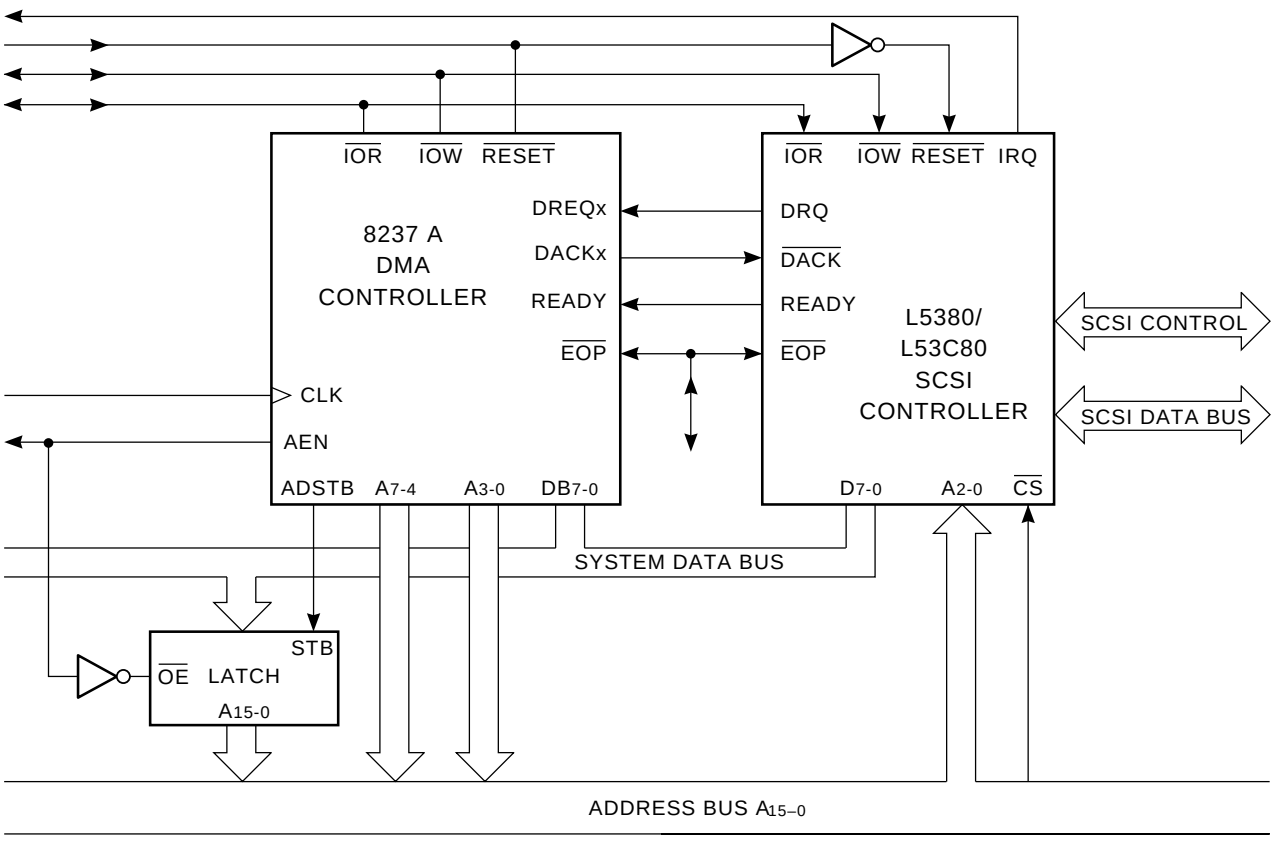
Mode	**Temperature Range** (Ambient)	**Supply Voltage**
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ **V**CC ≤ 5.25 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VIL	Input Low Voltage		0.0		0.8	V
VIH	Input High Voltage		2.0		**V**CC	V
VOL	Output Low Voltage (SCSI bus)	**V**CC = Min, **I**OL = 48 mA			0.5	V
VOL	Output Low Voltage (other pins)	**V**CC = Min, **I**OL = 8 mA			0.5	V
VOH	Output High Voltage (other pins)	**V**CC = Min, **I**OH = –4 mA	3.5			V
IIN	Input Current*	**V**CC = Max, **V**IN = 0 – **V**CC (SCSI bus)			65	µA
IIN	Input Current*	**V**CC = Max, **V**IN = 0 – **V**CC (other pins)			20	µA
ICC	Supply Current	**V**CC = Max, **V**IH = 2.4, VIL = 0.4, 4 MHz cycle, No Load, No Termination		10	20	mA
ICC	Supply Current Quiescent	Same as above, inputs stable			1.5	mA

*Not tested at low temperature extreme.

DMA Interface with 8237 A

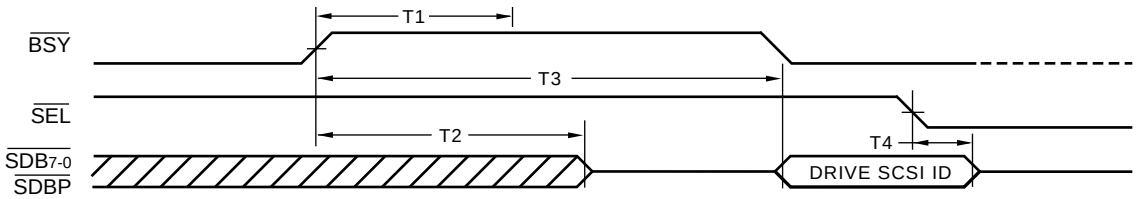


SWITCHING CHARACTERISTICS

Arbitration Timing *(ns — except where noted)*

Symbol	Parameter	L5380/53C80– Commercial Min	L5380/53C80– Commercial Max
T1	$\overline{BSY}$ False Duration to Detect Bus Free Condition	0.4 µs	1.2 µs
T2	SCSI Bus Clear (High Z) from $\overline{BSY}$ False		1.2 µs
T3	Arbitrate ($\overline{BSY}$ and SCSI ID Asserted) from $\overline{BSY}$ False (Bus Free Detected)	1.2 µs	2.2 µs
T4	SCSI Bus Clear (High Z) from $\overline{SEL}$ True (Lost Arbitration)		60

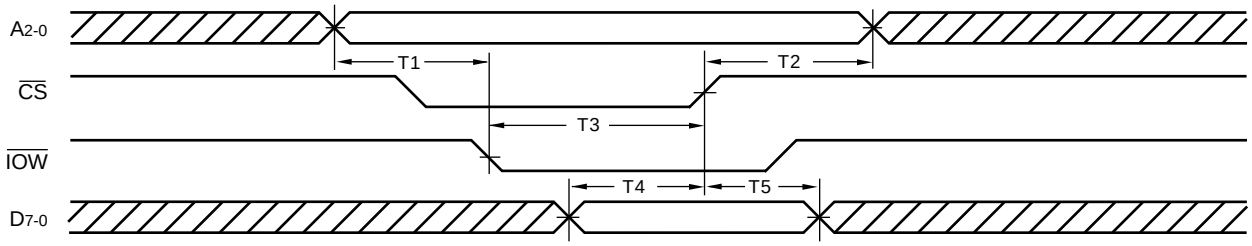
Arbitration Waveforms



CPU Write Cycle Timing *(ns)*

Symbol	Parameter	Commercial 2 Mbytes/sec Min	Commercial 2 Mbytes/sec Max	Commercial 4 Mbytes/sec Min	Commercial 4 Mbytes/sec Max
T1	Address Setup to Write Enable	10		5	
T2	Address Hold from End of Write Enable	5		5	
T3	Width of Write Enable	40		20	
T4	Data Setup to End of Write Enable	20		5	
T5	Data Hold from End of Write Enable	10		5	

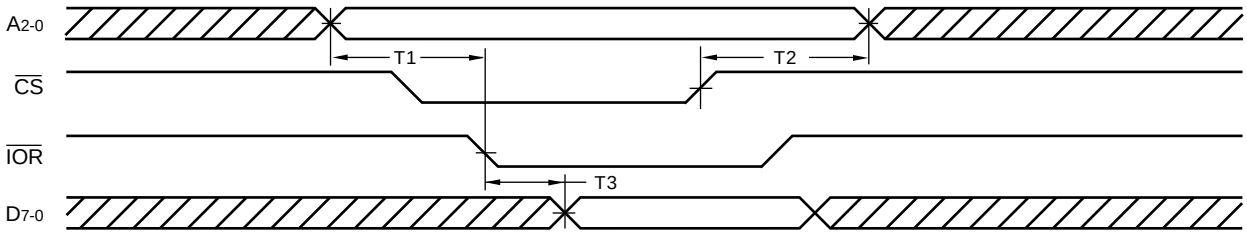
CPU Write Cycle Waveforms



CPU Read Cycle Timing *(ns)*

Symbol	Parameter	Commercial 2 Mbytes/sec Min	Commercial 2 Mbytes/sec Max	Commercial 4 Mbytes/sec Min	Commercial 4 Mbytes/sec Max
T1	Address Setup to Read Enable	10		5	
T2	Address Hold from End of Read Enable	5		5	
T3	Data Access Time from Read Enable		50		30

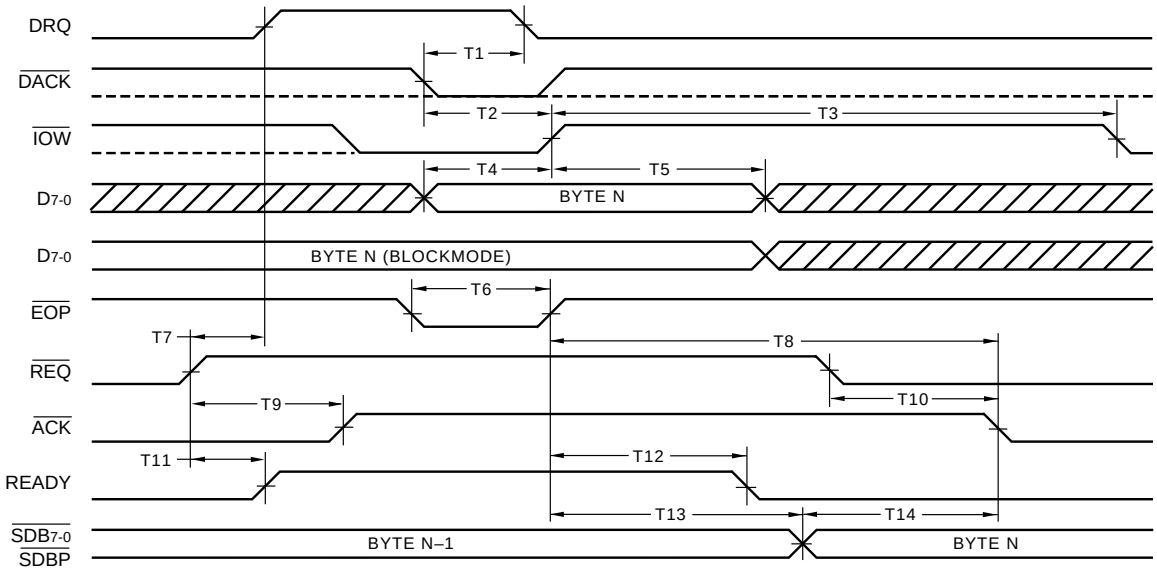
CPU Read Cycle Waveforms



DMA Write Initiator Send Timing *(ns)*

Symbol	Parameter	Commercial			
		2 Mbytes/sec		4 Mbytes/sec	
		Min	Max	Min	Max
	The following apply for all DMA Modes				
T1	DRQ False from Write Enable (concurrence of $\overline{IOW}$ and $\overline{DACK}$)		60		30
T2	Width of Write Enable (concurrence of $\overline{IOW}$ and $\overline{DACK}$)	60		20	
T4	Data Setup to End of Write Enable	20		5	
T5	Data Hold from End of Write Enable	15		5	
T6	Concurrent Width of $\overline{EOP}$, $\overline{IOW}$, and $\overline{DACK}$	50		20	
T9	$\overline{REQ}$ False to $\overline{ACK}$ False		90		45
T13	End of Write Enable to Valid SCSI Data		65		45
T14	SCSI Data Setup Time to $\overline{ACK}$ True	60		65	
	The following apply for Normal DMA Mode only				
T7	$\overline{REQ}$ False to DRQ True		60		30
T8	$\overline{DACK}$ False to $\overline{ACK}$ True ($\overline{REQ}$ True)		185		165
T10	$\overline{REQ}$ True to $\overline{ACK}$ True ($\overline{DACK}$ False)		70		35
	The following apply for Blockmode DMA only				
T3	$\overline{IOW}$ Recovery Time	40		20	
T8	$\overline{IOW}$ False to $\overline{ACK}$ True ($\overline{REQ}$ True)		185		165
T10	$\overline{REQ}$ True to $\overline{ACK}$ True ($\overline{IOW}$ False)		70		35
T11	$\overline{REQ}$ False to READY True		60		30
T12	$\overline{IOW}$ False to READY False		70		35

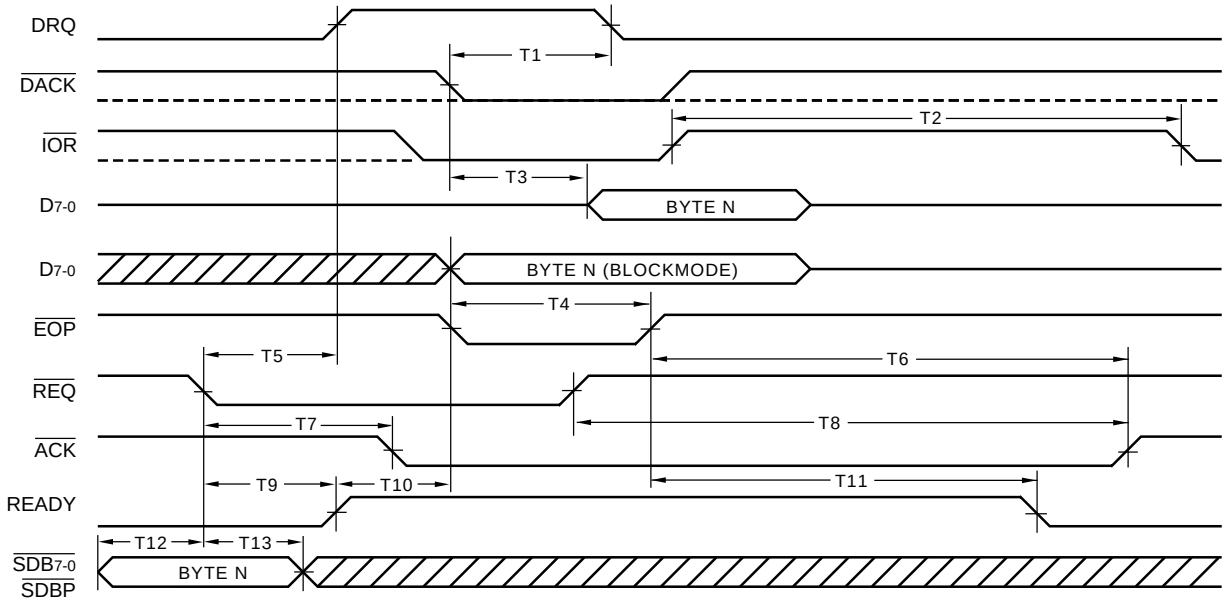
DMA Write Initiator Send Waveforms



DMA Read Initiator Receive Timing *(ns)*

Symbol	Parameter	Commercial			
		2 Mbytes/sec		4 Mbytes/sec	
		Min	Max	Min	Max
	The following apply for all DMA Modes				
T1	DRQ False from Concurrence of $\overline{IOR}$ and $\overline{DACK}$		60		30
T3	Data Access Time from Concurrence of $\overline{IOR}$ and $\overline{DACK}$		60		20
T4	Concurrent Width of $\overline{EOP}$, $\overline{IOR}$, and $\overline{DACK}$	50		20	
T7	$\overline{REQ}$ True to $\overline{ACK}$ True		70		35
T12	SCSI Data Setup Time to $\overline{REQ}$ True	20		5	
T13*	SCSI Data Hold Time from $\overline{REQ}$ True	15		10	
	The following apply for Normal DMA Mode only				
T5	$\overline{REQ}$ True to DRQ True		60		30
T6	$\overline{DACK}$ False to $\overline{ACK}$ False ($\overline{REQ}$ False)		90		55
T8	$\overline{REQ}$ False to $\overline{ACK}$ False ($\overline{DACK}$ False)		80		55
	The following apply for Blockmode DMA only				
T2	$\overline{IOR}$ Recovery Time	40		20	
T6	$\overline{IOR}$ False to $\overline{ACK}$ False ($\overline{REQ}$ False)		90		45
T8	$\overline{REQ}$ False to $\overline{ACK}$ False ($\overline{IOR}$ False)		80		45
T9	$\overline{REQ}$ True to READY True		60		30
T10	READY True to CPU Data Valid		15		15
T11	$\overline{IOR}$ False to READY False		70		35

DMA Read Initiator Receive Waveforms

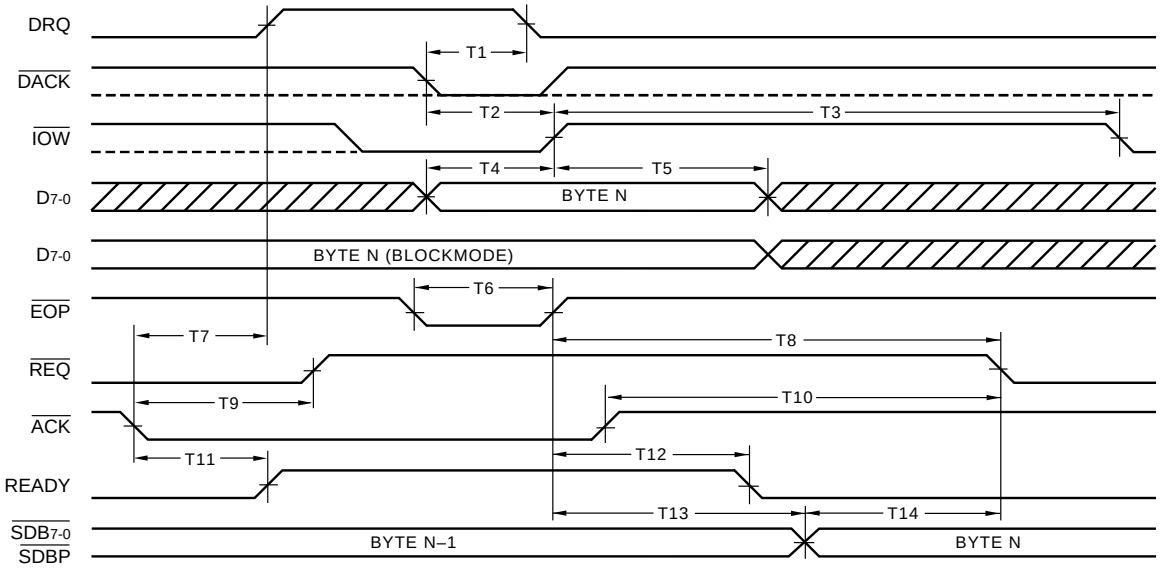


*Data must be held on the SCSI bus until $\overline{ACK}$ becomes True

DMA Write Target Send Timing *(ns)*

Symbol	Parameter	Commercial 2 Mbytes/sec Min	Commercial 2 Mbytes/sec Max	Commercial 4 Mbytes/sec Min	Commercial 4 Mbytes/sec Max
	The following apply for all DMA Modes				
T1	DRQ False from Write Enable (concurrence of $\overline{IOW}$ and $\overline{DACK}$)		60		30
T2	Width of Write Enable (concurrence of $\overline{IOW}$ and $\overline{DACK}$)	60		20	
T4	Data Setup to End of Write Enable	20		5	
T5	Data Hold from End of Write Enable	15		5	
T6	Concurrent Width of $\overline{EOP}$, $\overline{IOW}$, and $\overline{DACK}$	50		20	
T9	$\overline{ACK}$ True to $\overline{REQ}$ False		90		45
T13	End of Write Enable to Valid SCSI Data		60		45
T14	SCSI Data Setup Time to $\overline{REQ}$ True	60		65	
	The following apply for Normal DMA Mode only				
T7	$\overline{ACK}$ True to DRQ True		60		30
T8	$\overline{DACK}$ False to $\overline{REQ}$ True ($\overline{ACK}$ False)		185		165
T10	$\overline{ACK}$ False to $\overline{REQ}$ True ($\overline{DACK}$ False)		70		35
	The following apply for Blockmode DMA only				
T3	$\overline{IOW}$ Recovery Time	40		20	
T8	$\overline{IOW}$ False to $\overline{REQ}$ True ($\overline{ACK}$ False)		185		165
T10	$\overline{ACK}$ False to $\overline{REQ}$ True ($\overline{IOW}$ False)		70		35
T11	$\overline{ACK}$ True to READY True		60		30
T12	$\overline{IOW}$ False to READY False		70		35

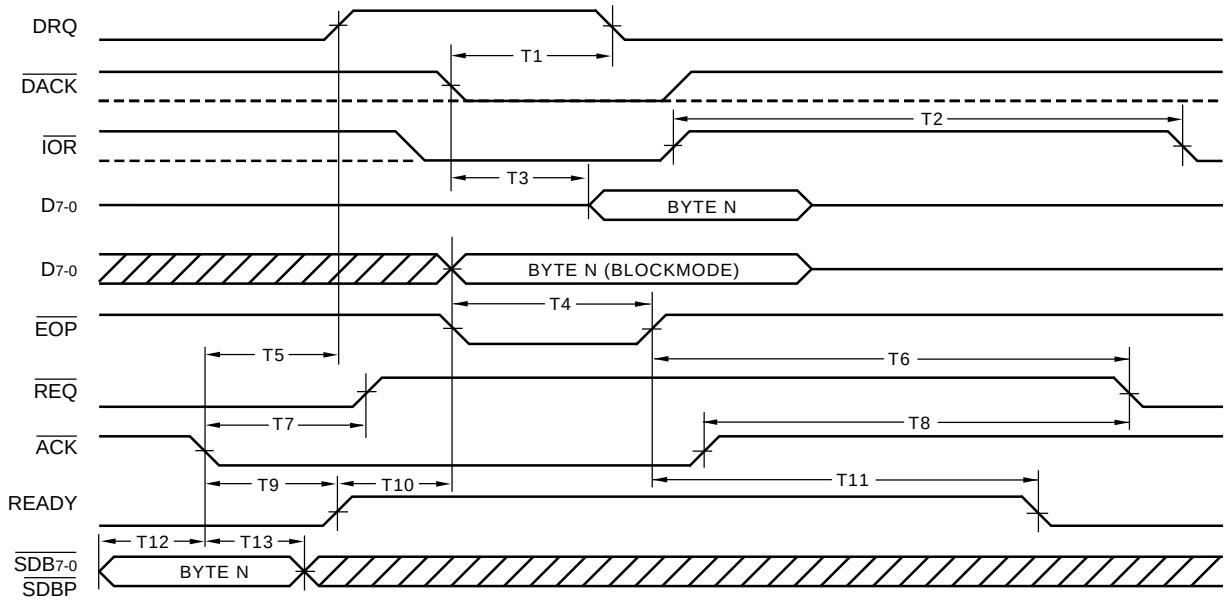
DMA Write Target Send Waveforms



DMA Read Target Receive Timing *(ns)*

Symbol	Parameter	Commercial			
		2 Mbytes/sec		4 Mbytes/sec	
		Min	Max	Min	Max
The following apply for all DMA Modes					
T1	DRQ False from Concurrence of $\overline{IOR}$ and $\overline{DACK}$		60		30
T3	Data Access Time from Concurrence of $\overline{IOR}$ and $\overline{DACK}$		60		20
T4	Concurrent Width of $\overline{EOP}$, $\overline{IOR}$, and $\overline{DACK}$	50		20	
T7	$\overline{ACK}$ True to $\overline{REQ}$ False		70		45
T12	SCSI Data Setup Time to $\overline{ACK}$ True	20		10	
T13*	SCSI Data Hold Time from $\overline{ACK}$ True	15		10	
The following apply for Normal DMA Mode only					
T5	$\overline{ACK}$ True to DRQ True		60		30
T6	$\overline{DACK}$ False to $\overline{REQ}$ True ($\overline{ACK}$ False)		90		45
T8	$\overline{ACK}$ False to $\overline{REQ}$ True ($\overline{DACK}$ False)		80		45
The following apply for Blockmode DMA only					
T2	$\overline{IOR}$ Recovery Time	40		20	
T6	$\overline{IOR}$ False to $\overline{REQ}$ True ($\overline{ACK}$ False)		90		45
T8	$\overline{ACK}$ False to $\overline{REQ}$ True ($\overline{IOR}$ False)		80		45
T9	$\overline{ACK}$ True to READY True		60		30
T10	READY True to CPU Data Valid		15		15
T11	$\overline{IOR}$ False to READY False		70		35

DMA Read Target Receive Waveforms



*Data must be held on the SCSI bus until $\overline{REQ}$ becomes False

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

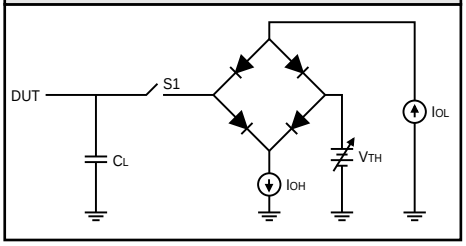
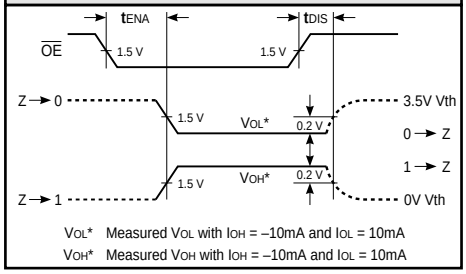
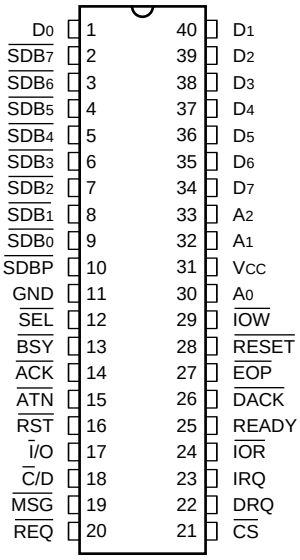


FIGURE B. THRESHOLD LEVELS

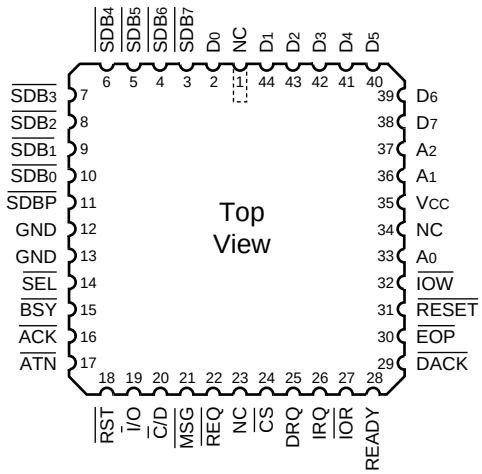


L5380 — ORDERING INFORMATION

40-pin — 0.6" wide



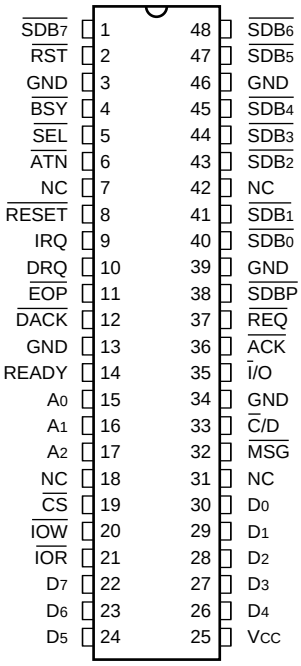
44-pin



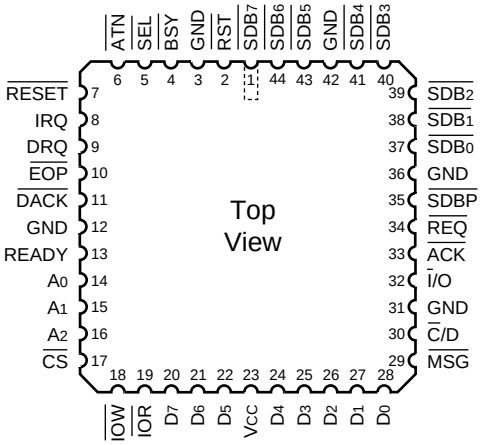
Speed	Plastic DIP (P3)	Plastic J-Lead Chip Carrier (J1)
	0°C to +70°C — COMMERCIAL SCREENING	
4	L5380PC4	L5380JC4
2	L5380PC2	L5380JC2

L53C80 — ORDERING INFORMATION

48-pin



44-pin



Speed	Plastic DIP (P5)	Sidebraze Hermetic DIP (D5)	Plastic J-Lead Chip Carrier (J1)
	0°C to +70°C — COMMERCIAL SCREENING		
4	L53C80PC4	L53C80DC4	L53C80JC4
2	L53C80PC2	L53C80DC2	L53C80JC2