

DESCRIPTION

The NN514256 series is a high performance CMOS Dynamic Random Access Memory organized as 262,144 words by 4 bits. The NN514256 series is fabricated with advanced CMOS technology and designed with innovative design techniques resulting in high speed, extremely low power and wide operating margins at both component and system levels.

The NN514256 series features a high speed page mode operation in which a high speed read, write or read-write is performed on any column address along a row address.

An extremely short row address capture time and an asynchronous column address decoder relax the timing constraints associated with address multiplexing.

The outputs are tri-stated by $\overline{\text{CAS}}$ which, in essence, acts as an output enable independent of $\overline{\text{RAS}}$ with very fast CAS to output access time.

Refresh is accomplished by performing $\overline{\text{RAS}}$ only refresh cycles, hidden refresh cycles, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles, or normal read or write cycles on the 512 address combinations of A0 to A8 during a 8 ms period.

Multiplexed address inputs permit The NN514256 series to be packaged in a standard 20-pin plastic DIP, 26-pin plastic SOJ, 20-pin plastic ZIP and 24 pin TSOP TYPE I. The package sizes provide high system bit densities and are compatible with widely available automated testing and insertion equipment. System level features include single power supply of 5V ±10% tolerance and direct interface with high performance TTL logic families.

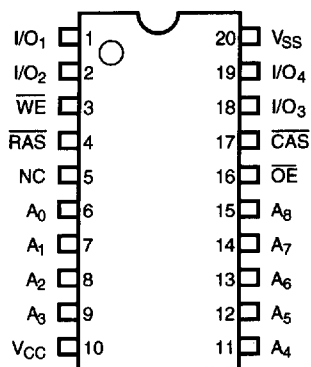
FEATURES

- 262,144 × 4 bit Organization
- Single 5V ±10% Power Supply
- Performance Ranges

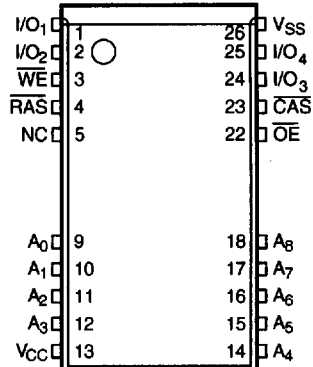
Parameter	-40	-45	-50	-60	-70
Max. $\overline{\text{RAS}}$ Access Time (t_{RAC})	40ns	45ns	50ns	60ns	70ns
Max. $\overline{\text{CAS}}$ Access Time (t_{CAC})	13ns	15ns	15ns	15ns	20ns
Max. Column Address Access Time (t_{AA})	25ns	25ns	27ns	30ns	35ns
Min. Read/Write Cycle Time (t_{RC})	80ns	80ns	90ns	110ns	130ns

- Fast Page Mode Operation
- Low Power Operation
 - Low Standby Current (CMOS level inputs)
 - Standard 1mA
 - L version 50μA
- 512 Refresh Cycles
 - Standard distributed across 8ms
 - L version distributed across 128ms
- All inputs/Outputs and Clocks fully TTL and CMOS compatible
- Refresh Modes
 - $\overline{\text{RAS}}$ only
 - $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$
 - Hidden Refresh
- High Reliability Packages
 - Plastic 20pin DIP (P20DP-1A0)
 - Plastic 20pin ZIP (P20ZP-2B0)
 - Plastic 26pin SOJ (P26SJ-2A6)
 - Plastic 24pin TSOP TYPE I (P24TV-5B4)

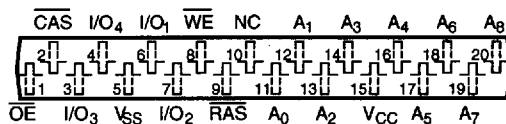
PIN CONFIGURATION (TOP VIEW)



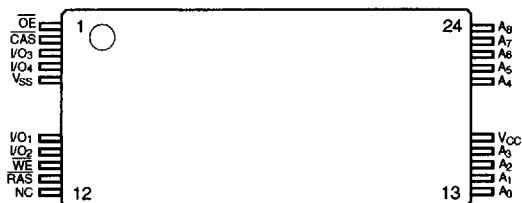
20-pin DIP (300mil)
P20DP-1A0



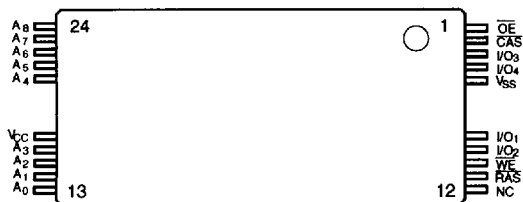
20/26-pin SOJ (300mil)
P26SJ-2A6



20-pin ZIP (400mil)
P20ZP-2B0



20/24-pin TSOP TYPE (I)
Normal Bend (6×16mm)
P24TV-5B4

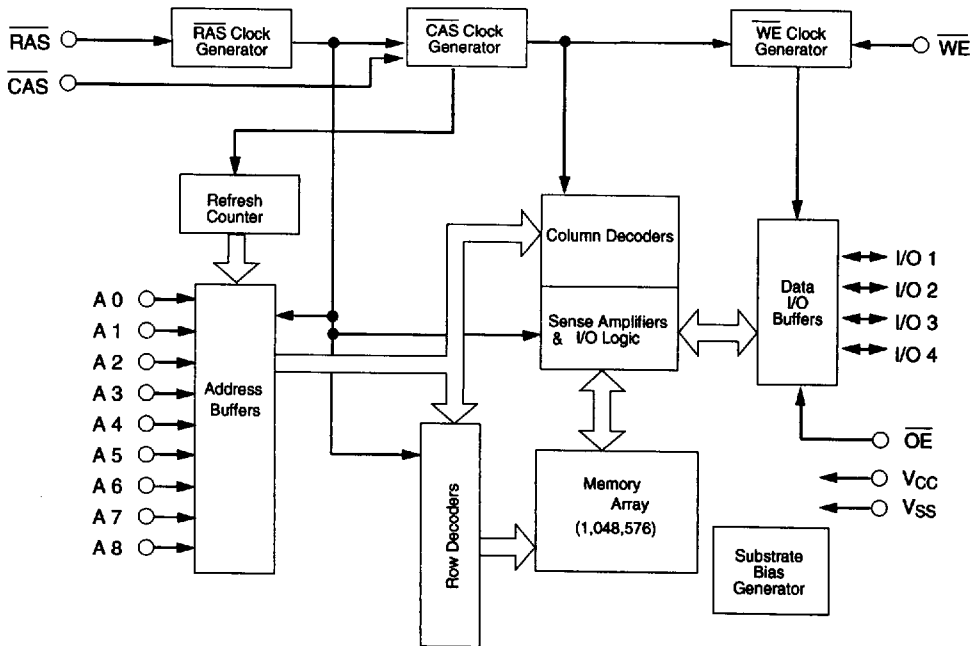


20/24-pin TSOP TYPE (I)
Reverse Bend (6×16mm)
P24TV-5B4-R

PIN NAMES

A0~A8	Address Inputs
RAS	Row Address Strobe
CAS	Column Address Strobe
OE	Output Enable
I/O1~I/O4	Data-in / Data-out
WE	Write Enable
V _{CC}	+5V Supply
V _{SS}	Ground
NC	No Connection

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	VALUE	UNIT
Voltage on Any Pin Relative to V_{SS}	V_{in}, V_{out}	-1 to 7	V
Voltage on V_{CC} Relative to V_{SS}	V_{CC}	-1 to 7	V
Storage Temperature (Plastic)	T_{stg}	-55 to +125	°C
Power Dissipation	P_d	1.0	W
Ambient Operating Temperature	T_a	0 to +70	°C
Short Circuit Output Current	I_{out}	50	mA

Permanent device damage can occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage, All Inputs	2.4	—	6.5	V
V_{IL}	Input Low Voltage, All Inputs	-1.0	—	0.8	V

Note: All voltage values in this data sheet are with respect to V_{SS} unless otherwise specified.

DC ELECTRICAL CHARACTERISTICS (0°C ≤ Ta ≤ 70°C, V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	SPEED	MIN.	MAX.	UNIT	TEST CONDITIONS	NOTES
I _{CC1}	Operating Current	-40 -45 -50 -60 -70		110 100 90 80 70	mA mA mA mA mA	t _{RC} = t _{RC} (min.) RAS, CAS, Address cycling	1, 2
I _{CC2}	Standby Current			1.0	mA	RAS = CAS ≥ (V _{CC} - 0.2V)	
				2.0	mA	RAS = CAS ≥ V _{IH}	
	Standby Current (L version)			50	μA	RAS = CAS ≥ (V _{CC} - 0.2V) All other inputs are stable at (V _{CC} - 0.2V) or (V _{SS} + 0.2V)	
I _{CC3}	Refresh Current (RAS only refresh)	-40 -45 -50 -60 -70		110 100 90 80 70	mA mA mA mA mA	t _{RC} = t _{RC} (min.) RAS cycling, CAS = V _{IH}	1
I _{CC4}	Fast Page Mode Current	-40 -45 -50 -60 -70		80 80 70 60 50	mA mA mA mA mA	t _{PC} = t _{PC} (min.) RAS = V _{IL} CAS, Address cycling	1, 2
I _{CC5}	Refresh Current (CAS before RAS refresh)	-40 -45 -50 -60 -70		110 100 90 80 70	mA mA mA mA mA	t _{RC} = t _{RC} (min.) RAS, CAS cycling	1
I _{CC6}	Refresh Current (L version : CAS before RAS refresh)			150	μA	512 cycles / 128ms t _{RAS} ≤ 200ns, WE ≥ (V _{CC} - 0.2V) All other inputs are stable at (V _{CC} - 0.2V) or (V _{SS} + 0.2V)	
I _{L1}	Input Leakage Current (Any input pin)		-10	10	μA	0V ≤ V _{IH} ≤ 5.5V, Others = 0V	
I _{L0}	Output Leakage Current (For high impedance state)		-10	10	μA	RAS ≥ V _{IH} (min.), CAS ≥ V _{IH} (min.) 0V ≤ V _{OUT} ≤ 5.5V	
V _{OH}	Output High Voltage		2.4		V	I _{OH} = -5.0 mA	
V _{OL}	Output Low Voltage			0.4	V	I _{OL} = 4.2 mA	

Notes: 1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rate.

2. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the outputs open.

CAPACITANCE (0°C ≤ Ta ≤ 70°C, V_{CC} = 5.0V ±10%, f = 1MHz)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C _{IN1}	Address(A0 ~ A8)	—	5	pF
C _{IN2}	RAS, CAS, WE, OE	—	5	pF
C _{OUT}	I/O1, I/O2, I/O3, I/O4	—	7	pF

A.C. OPERATING CONDITIONS (0 °C ≤ Ta ≤ 70 °C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) (NOTES 3, 4, 5)

NO.	NOTES		PARAMETER	-40		-45		-50		-60		-70		UNIT	NOTE
	JEDEC	STD.		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t _{CL1QV}	t _{CAC}	Access Time from CAS	—	13	—	15	—	15	—	15	—	20	ns	6,13
2	t _{CH2QV}	t _{CPA}	Access Time from CAS Precharge	—	30	—	30	—	32	—	35	—	40	ns	13,14
3	t _{AVQV}	t _{AA}	Access Time from Column Address	—	25	—	25	—	27	—	30	—	35	ns	7,13
4	t _{RL1QV}	t _{RAC}	Access Time from RAS	—	40	—	45	—	50	—	60	—	70	ns	6,7
5	t _{RL1CH1}	t _{CSH}	CAS Hold Time	40	—	45	—	50	—	60	—	70	—	ns	
6	t _{RL1CH1}	t _{CHR}	CAS Hold Time (CAS before RAS Refresh)	10	—	10	—	10	—	10	—	10	—	ns	
7	t _{CH2CL2}	t _{CPN}	CAS Precharge Time (CAS before RAS Refresh)	10	—	10	—	10	—	10	—	10	—	ns	
8	t _{CH2CL2}	t _{CPT}	CAS Precharge Time	10	—	10	—	10	—	10	—	10	—	ns	
9	t _{CH2CL2}	t _{CP}	CAS Precharge Time (Fast Page Mode)	5	—	5	—	5	—	5	—	5	—	ns	14
10	t _{CL1CH1}	t _{CAS}	CAS Pulse Width	15	100K	15	100K	15	100K	15	100K	20	100K	ns	
11	t _{CL1RL2}	t _{CSR}	CAS Setup Time (CAS before RAS Refresh)	5	—	5	—	5	—	5	—	5	—	ns	
12	t _{CL1OX}	t _{CLZ}	CAS to Output in Low-Z	0	—	0	—	0	—	0	—	0	—	ns	8
13	t _{CH2RL2}	t _{CRP}	CAS to RAS Precharge Time	5	—	5	—	5	—	5	—	5	—	ns	
14	t _{CL1WL2}	t _{CWD}	CAS to WE Delay Time	45	—	45	—	45	—	45	—	50	—	ns	11
15	t _{CL1AX}	t _{CAH}	Column Address Hold Time	10	—	10	—	10	—	15	—	15	—	ns	
16	t _{RL1AX}	t _{AR}	Column Address Hold Time Referenced to RAS	30	—	30	—	35	—	40	—	40	—	ns	
17	t _{AVCL2}	t _{ASC}	Column Address Setup Time	0	—	0	—	0	—	0	—	0	—	ns	14
18	t _{AVRH1}	t _{RAL}	Column Address to RAS Lead Time	25	—	25	—	27	—	30	—	35	—	ns	
19	t _{AVWL2}	t _{AWD}	Column Address to WE Delay Time	55	—	55	—	57	—	60	—	65	—	ns	11
20	t _{CL1DX} t _{WL1DX}	t _{DH}	Data Hold Time	10	—	10	—	10	—	10	—	10	—	ns	12
21	t _{DVCL2} t _{DVWL2}	t _{DS}	Data Setup Time	0	—	0	—	0	—	0	—	0	—	ns	12
22	t _{OL1QV}	t _{OEa}	OE Access Time	—	15	—	15	—	15	—	15	—	20	ns	
23	t _{WL1OL2}	t _{OEh}	OE Command Hold Time	15	—	15	—	15	—	15	—	20	—	ns	
24	t _{CH2QV}	t _{OED}	OE to Data Delay Time	10	—	10	—	10	—	10	—	10	—	ns	
25	t _{CH2QZ}	t _{OFF}	Output Buffer Turn-off Delay Time	0	13	0	13	0	13	0	15	0	20	ns	10
26	t _{OH2QX}	t _{OEZ}	Output Buffer Turn-off Delay Time Referenced to OE	0	10	0	10	0	10	0	15	0	15	ns	
27	t _{CL1RH1}	t _{RSH}	RAS Hold Time	15	—	15	—	15	—	15	—	20	—	ns	
28	t _{OL1RH1}	t _{ROH}	RAS Hold Time Referenced to OE	10	—	10	—	10	—	10	—	10	—	ns	
29	t _{RH2RL2}	t _{RP}	RAS Precharge Time	25	—	25	—	25	—	30	—	40	—	ns	
30	t _{RL1RH1}	t _{RAS}	RAS Pulse Width	40	100K	45	100K	50	100K	60	100K	70	100K	ns	
31	t _{RL1RH1}	t _{RASP}	RAS Pulse Width (Fast Page Mode)	40	100K	45	100K	50	100K	60	100K	70	100K	ns	
32	t _{RL1CL1}	t _{RCD}	RAS to CAS Delay Time	13	25	13	30	13	35	13	45	13	50	ns	6
33	t _{RH2CL2}	t _{RPC}	RAS to CAS Precharge Time	10	—	10	—	10	—	10	—	10	—	ns	
34	t _{RL1AV}	t _{RAD}	RAS to Column Address Delay Time	11	15	11	20	11	23	11	30	11	35	ns	7
35	t _{RL1WL2}	t _{RWD}	RAS to WE Delay Time	70	—	75	—	80	—	90	—	100	—	ns	11
36	t _{CH2WL2}	t _{RCH}	Read Command Hold Time	0	—	0	—	0	—	0	—	0	—	ns	9
37	t _{RH2WL2}	t _{RRH}	Read Command Hold Time Referenced to RAS	10	—	10	—	10	—	10	—	10	—	ns	9
38	t _{WH2CL2}	t _{RCS}	Read Command Setup Time	0	—	0	—	0	—	0	—	0	—	ns	

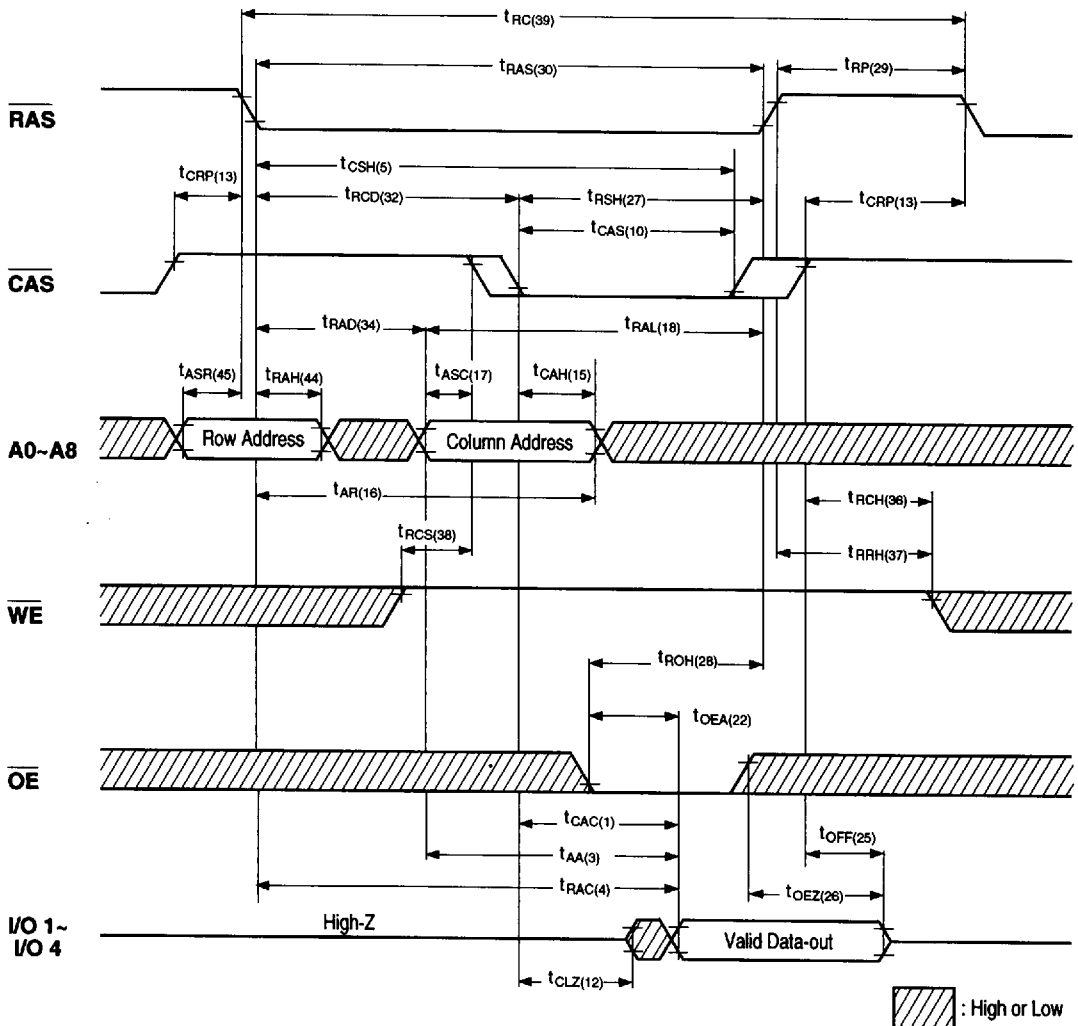
NN514256 series
CMOS 256K × 4bit Dynamic RAM

NO.	SYMBOL		PARAMETER	-40		-45		-50		-60		-70		UNIT	NOTE
	JEDEC	STD.		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
39	t _{RL2RL2}	t _{RC}	Random Read or Write Cycle Time	80	—	80	—	90	—	110	—	130	—	ns	
40	t _{CL2CL2}	t _{PC}	Read or Write Cycle Time (Fast Page Mode)	30	—	30	—	33	—	40	—	45	—	ns	13,14
41	t _{RL2RL2}	t _{RMW}	Read-Modify-Write Cycle Time	130	—	135	—	145	—	165	—	185	—	ns	
42	t _{CL2CL2}	t _{PRMW}	Read-Modify-Write Cycle Time (Fast Page Mode)	85	—	90	—	90	—	95	—	100	—	ns	13,14
43	t _{REF}	t _{REF}	Refresh Period	—	8	—	8	—	8	—	8	—	8	ms	15
44	t _{RL1AX}	t _{RAH}	Row Address Hold Time	8	—	8	—	8	—	8	—	8	—	ns	
45	t _{AVRL2}	t _{ASR}	Row Address Setup Time	0	—	0	—	0	—	0	—	0	—	ns	
46	t _T	t _T	Transition Time (Rise and Fall)	2	50	2	50	2	50	2	50	2	50	ns	4,5
47	t _{CL1WH1}	t _{WCH}	Write Command Hold Time	10	—	10	—	10	—	10	—	15	—	ns	
48	t _{WL1WH1}	t _{WP}	Write Command Pulse Width	10	—	10	—	10	—	10	—	15	—	ns	
49	t _{WL1CL2}	t _{WCS}	Write Command Setup Time	0	—	0	—	0	—	0	—	0	—	ns	11
50	t _{WL1CH1}	t _{CWL}	Write Command to $\overline{\text{CAS}}$ Lead Time	10	—	15	—	15	—	15	—	20	—	ns	
51	t _{WL1RH1}	t _{RWL}	Write Command to $\overline{\text{RAS}}$ Lead Time	10	—	15	—	15	—	15	—	20	—	ns	

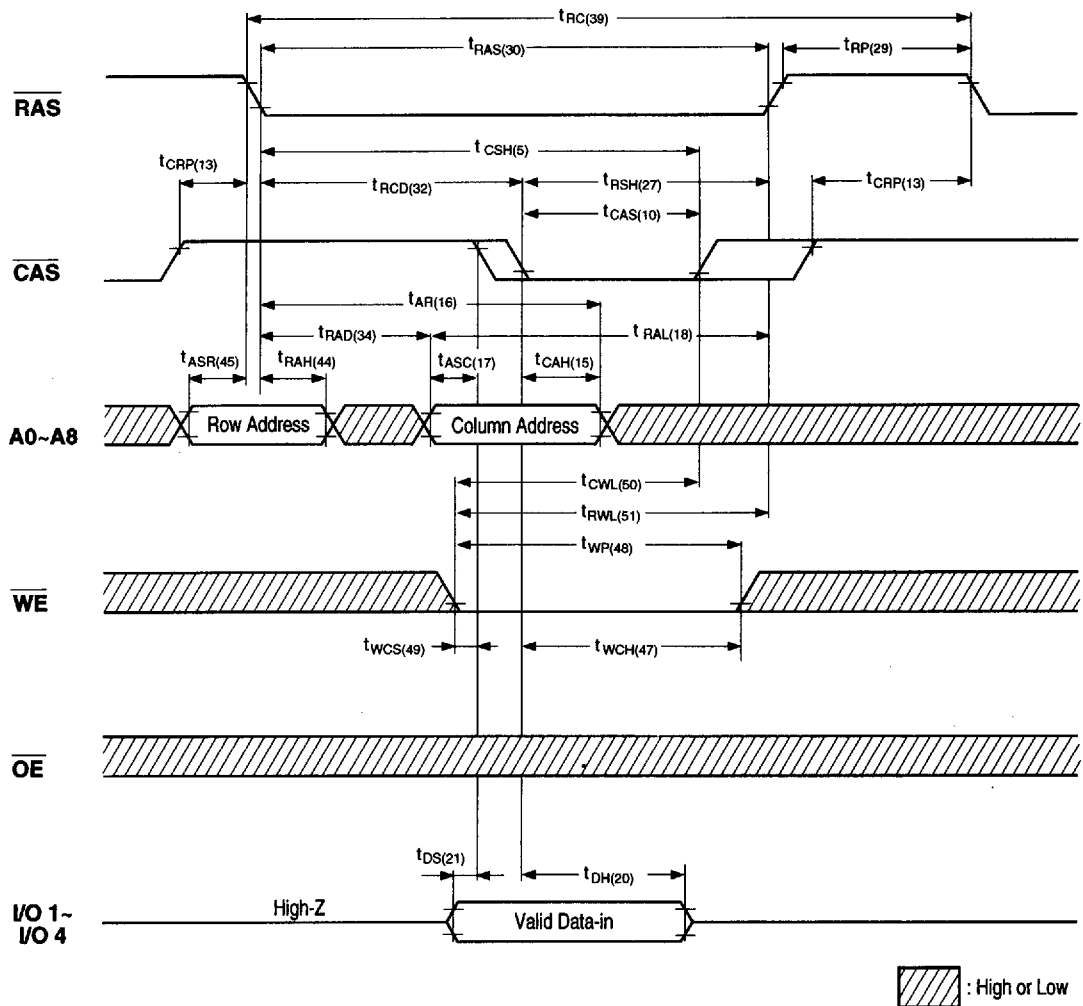
Notes:

- Eight Initialization Cycles are required following a 200 μ s pause after Power Up. These Initialization Cycles may consist of one of the following : $\overline{\text{RAS}}$ only refresh Cycles, Read Cycles, Write Cycles, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh Cycles.
- AC measurements assume $t_T=3$ ns. All AC parameters are measured with $V_{IL}(\text{min.}) \geq V_{SS}$ and $V_{IH}(\text{max.}) \leq V_{CC}$ and with a load equivalent to two TTL loads and 100pF.
- $V_{IH}(\text{min.})$ and $V_{IL}(\text{max.})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
- Operation within the $t_{RCD}(\text{max.})$ limit ensures that $t_{RAC}(\text{max.})$ can be met. $t_{RCD}(\text{max.})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\text{max.})$ limit, then access time is controlled by t_{CAC} .
- Operation within the $t_{RAD}(\text{max.})$ limit ensures that $t_{RAC}(\text{max.})$ can be met. $t_{RAD}(\text{max.})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\text{max.})$ limit, then access time is controlled by t_{AA} .
- Assumes three state test load (5pF and a 220 ohm to 1.3V Thevenin equivalent).
- Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
- $t_{OFF}(\text{max.})$ defines the time at which the output achieves an open circuit condition and is not referenced to output voltage levels.
- t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\text{min.})$, the cycle is an early write cycle and data-out pins will remain open circuit (high impedance) throughout the entire cycle. If $t_{RWD} \geq t_{RWD}(\text{min.})$, $t_{CWD} \geq t_{CWD}(\text{min.})$ and $t_{AWD} \geq t_{AWD}(\text{min.})$, the cycle is a read-modify-write cycle and the data-out will contain data read from the selected cell. If neither of the above conditions is satisfied, the condition of the data-out (at access time) is indeterminate.
- These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{WE}}$ leading edge in read-modify-write cycles.
- Access time is determined by the longer of t_{AA} , t_{CAC} , or t_{CPA} .
- $t_{ASC} \geq t_{CP}$ to achieve $t_{PC}(\text{min.})$ and $t_{CPA}(\text{max.})$ values.
- $t_{REF}=128$ msec for Long Refresh version (L version).

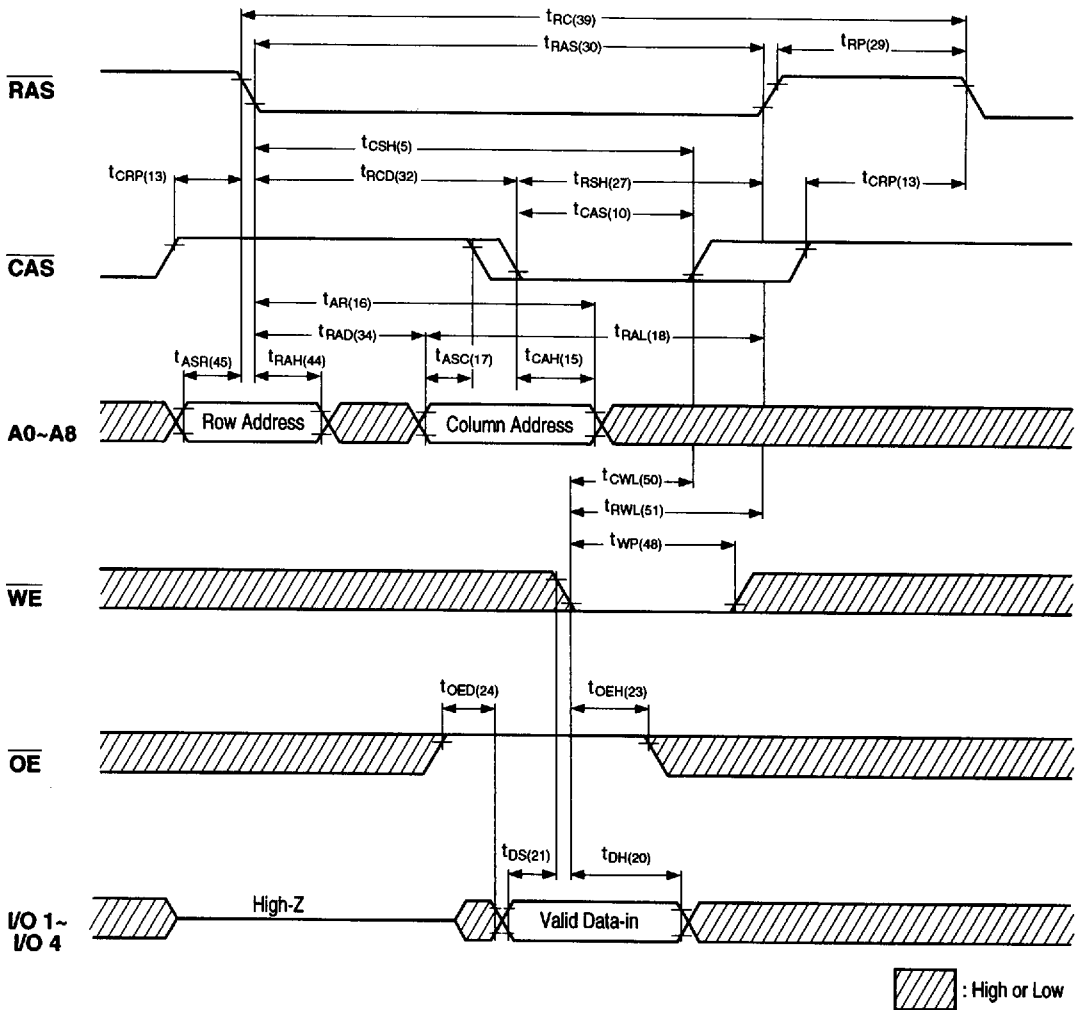
READ CYCLE



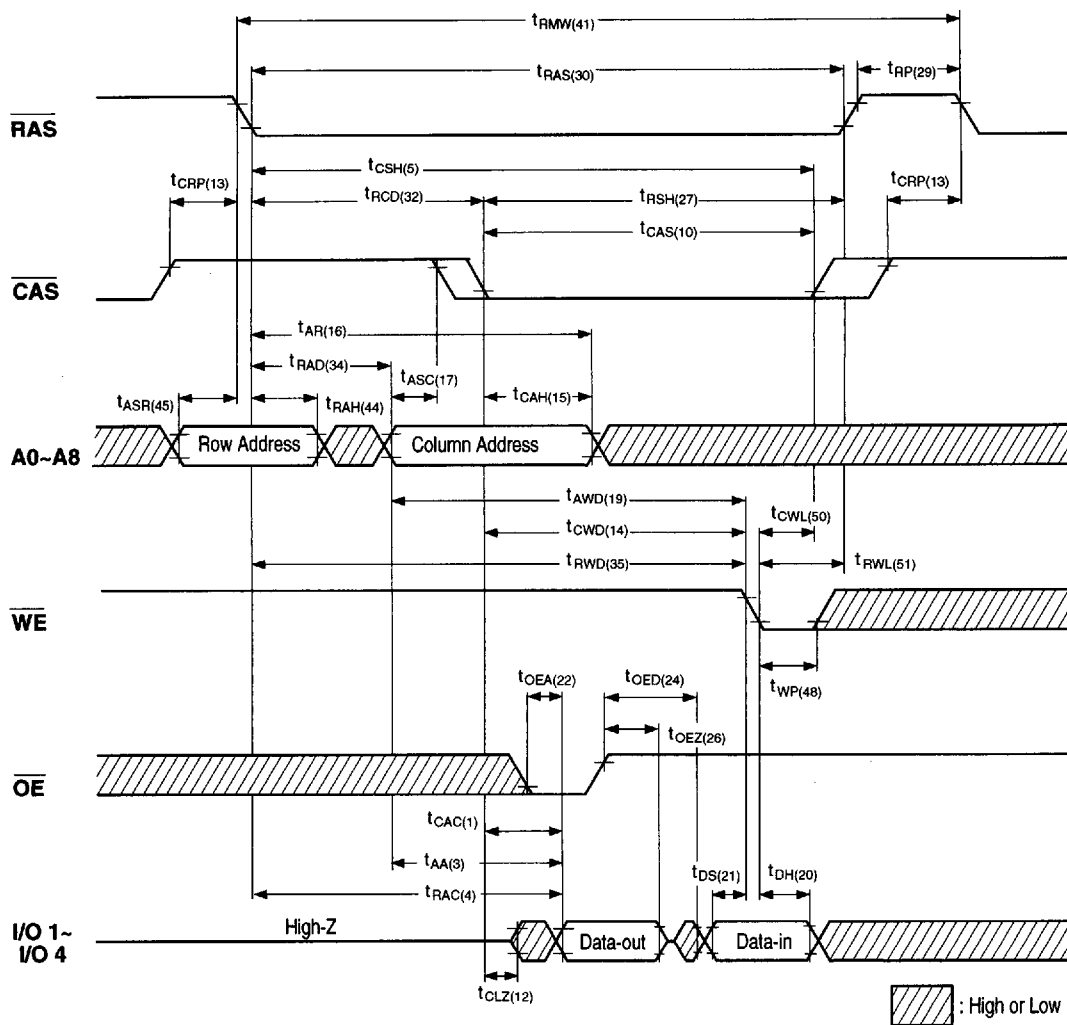
WRITE CYCLE (EARLY WRITE)



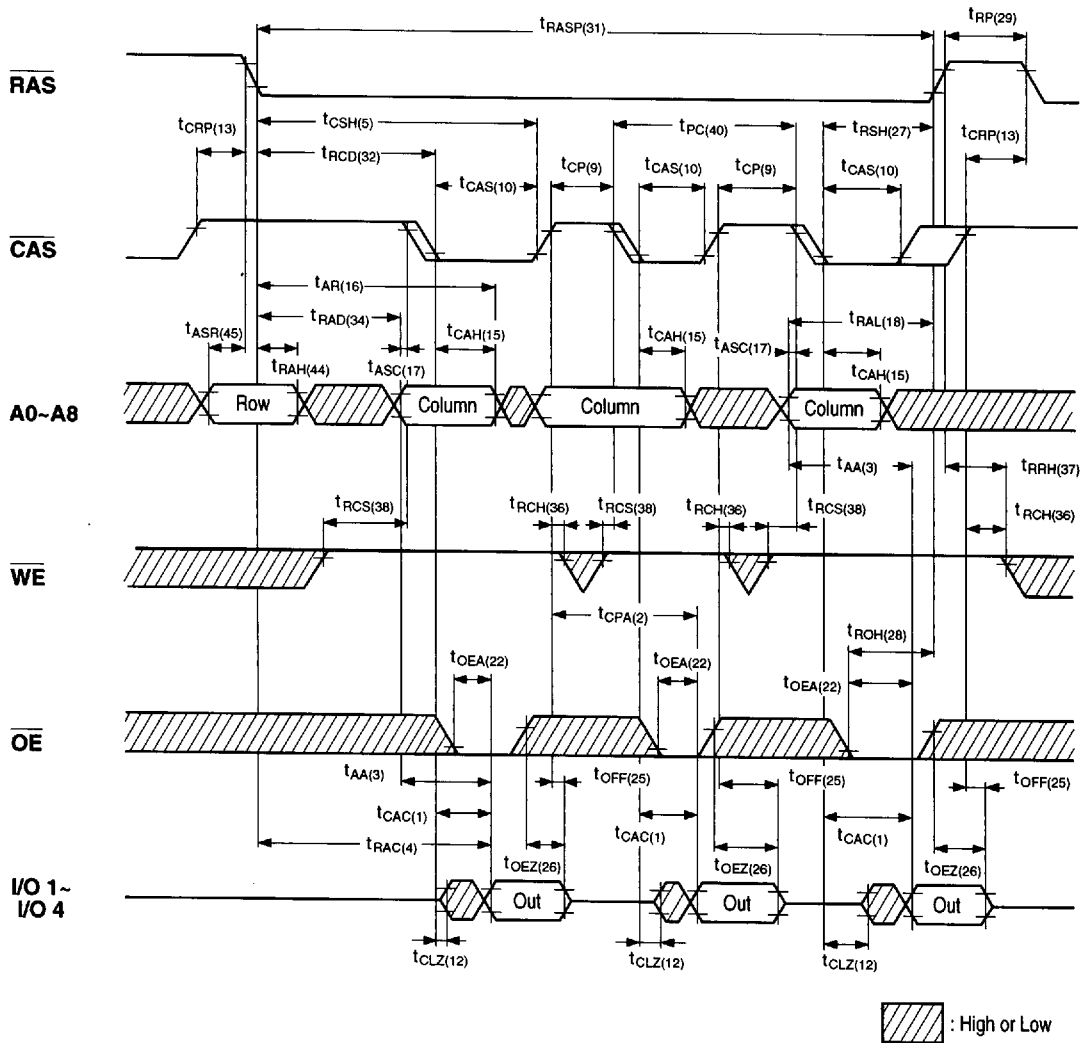
WRITE CYCLE (\overline{OE} -CONTROLLED WRITE)



READ-MODIFY-WRITE CYCLE



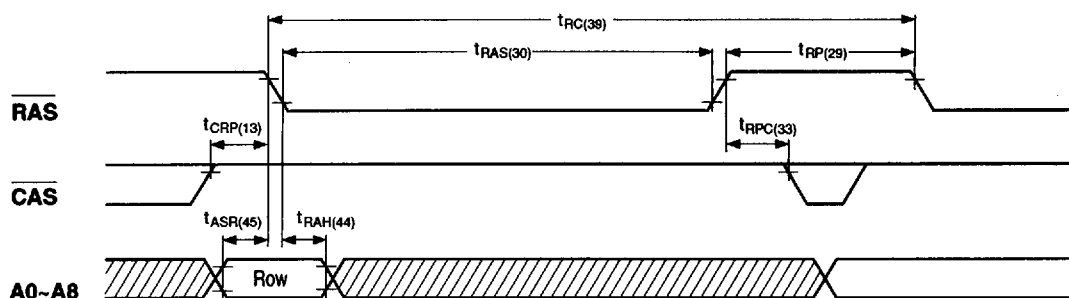
FAST PAGE MODE READ CYCLE







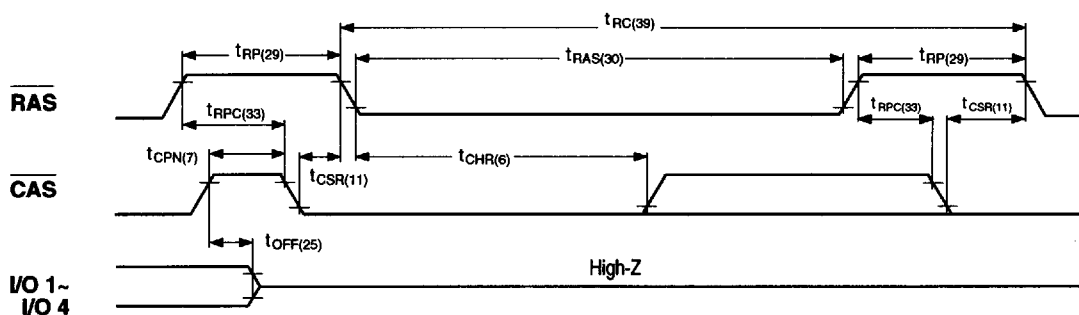
RAS ONLY REFRESH CYCLE



Note: \overline{WE} , \overline{OE} = Don't care.

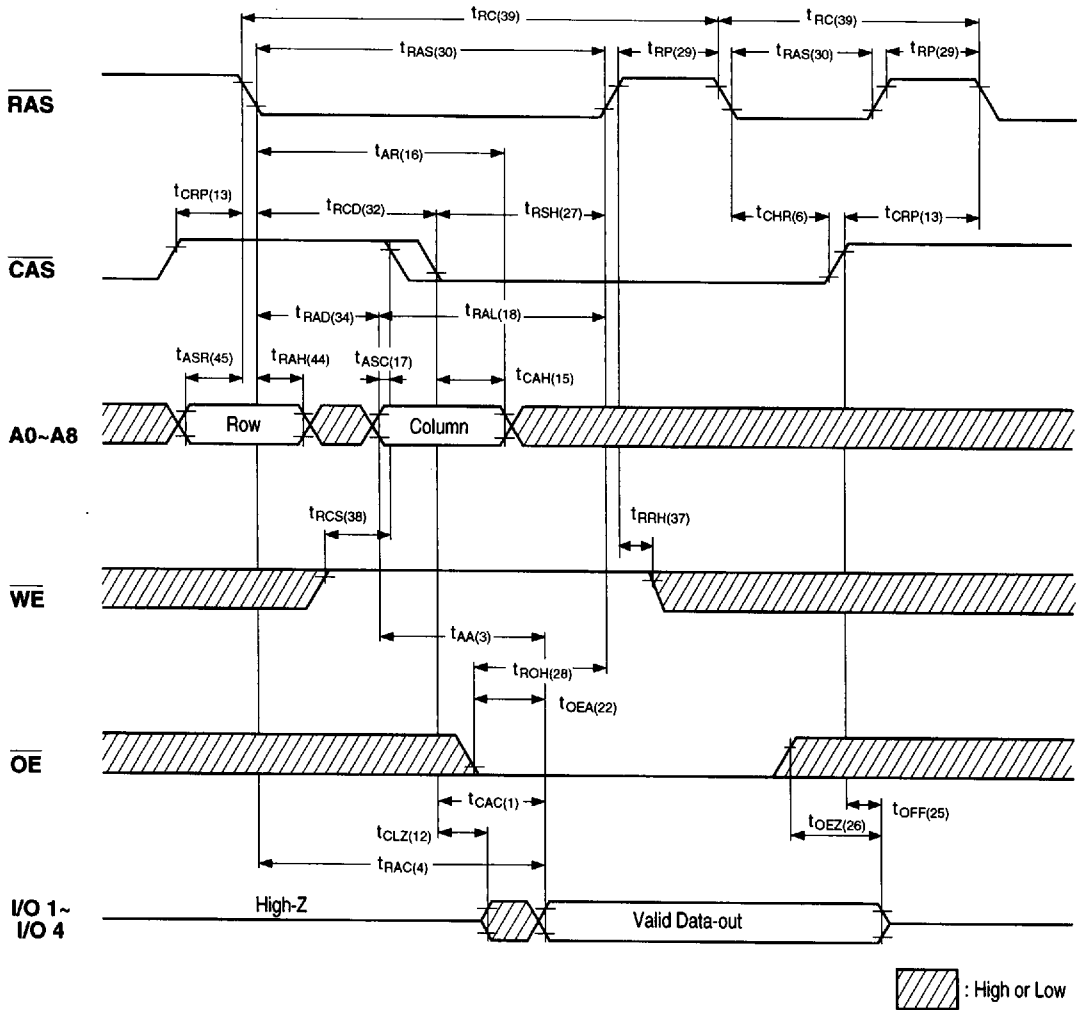
 : High or Low

CAS BEFORE RAS REFRESH CYCLE

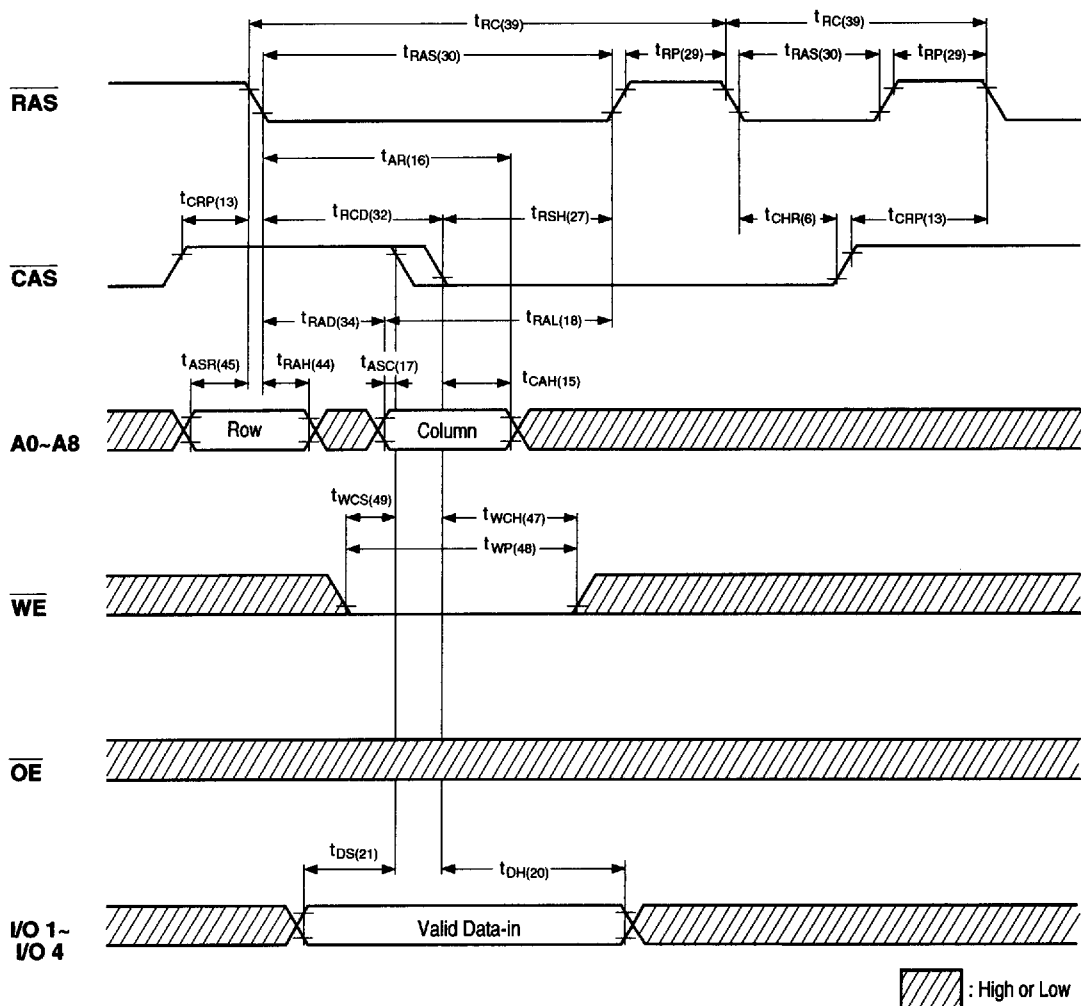


Note: \overline{OE} , A0~A8 = Don't care.

HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (EARLY WRITE)



ORDERING INFORMATION

NN514256XX - XX

SPEED	40	: 40ns
	45	: 45ns
	50	: 50ns
	60	: 60ns
PACKAGE	70	: 70ns
	P	: Plastic DIP
	J	: Plastic SOJ
	Z	: Plastic ZIP
VERSION	T	: Plastic TSOP TYPE I (Normal Bend)
	R	: Plastic TSOP TYPE I (Reverse Bend)
	BLANK	: Standard Version
	L	: Long Refresh Version 128ms Refresh
MODE	4256	: Fast Page 256K x 4