
Processor Replacement Card, Version 3
CPU Accelerator for the Atari ST(E) Series

# PAK68/3

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CPU Accelerator for the Atari ST(E) Series

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### Limitation of Liability

We reserve the right to make changes to the hardware, the GAL equations or the documentation withhout restriction. We are not responsible for the accuracy of the manual or damage resulting from the use of the hardware. Every modification done to your own computer system is performed at your own risk!

We are always grateful for suggestions to improve the manual.

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# 1. Before Starting

## 1.1 Notes

Please read the instructions carefully before you begin the construction and installation. Most errors can be attributed to an insuffucient knowledge of the instructions. The installation of the finished PAK68/3 board should be possible even for people with limited hardware experience. If the necessary steps seem too difficult, ask an acquaintance with some experience or contact us (see imprint).

Then again, anyone with the empty board or the parts kit shouldn't really face any great hurdles. The required steps are of medium difficulty so you should already have some experience with the construction and installation of circuit boards. The construction and installation of the PAK68/3 as well as changes to your computer are performed at your own risk.

The PAK68/3 was first introduced in the magazine c't. If you would like to read the articles they were in the 11/93 issue page 222 and the 12/93 issue page 276.

## 1.2 Delivery Options

The PAK68/3 is available in three versions; each with manual and disk.

- Empty board with optional programmed GALs
- Parts Kit (Empty board and hard to procure components)
- Ready-Built Unit

**optional:**

- PAK-GAL Set P13-50d, P2-ST, P3-PUK-A, V4-50ac, V5-51a, P6-ST (for operation without FRAK/?) or P6-F05 (for operation with FRAK/?). (GAL combinations at the time of the printing of the manual)

## 1.3 Requirements

The PAK is a very stable and trouble-free CPU accelerator but there are a few things to keep in mind:

- The PAK is designed to work only in 68000 based systems: i.e. not in the TT, Falcon or Clones.
- The target CPU package is DIP (64pin, rectangular). For PLCC-CPUs (STE, MSTE; 68pin, square) an adapter is needed since the PAK expects the CPU in DIP form. Unfortunately, this is a very problematic issue, since there are always problems with plug-type adapters. Therefore, we do not recommend installing the PAK in systems with PLCC-CPU.
- The CPU must already be socketed otherwise the PAK cannot be plugged in. If someone wants to use the 68000 CPU in alternate operating mode it can be used later on the PAK (together with the switchover GAL P3). The PAK cannot be installed onto an existing 68000 CPU!
- If a blitter is present it is best to completely remove it or at least disable it since it impedes the operation of the PAK. Incidentally, the PAK offers the speed benefits of the blitter anyway since it overtakes the performance of the blitter from 32MHz onwards.
- For the proper operation of the PAK a patched TOS 3.06 is necessary in EPROMs located on the PAK board. Without this PAK-TOS, if the PAK runs at all, it is very limited (because the PMMU of the 68030 is not initialized).
- The mainboard RAM should have a maximum access time of 100ns with 80ns being better and 60ns being optimal. Unfortunately, there are add-ons with 120ns and even 150ns. With those you will inevitably have problems (random crashes).
- If you run a TOS-Card (TOS 2.06 upgrade), you must check that the access time of any GALs present on the extension do not exceed 15ns. Unfortunately if the GAL used is slow (25ns for example), you must remove the TOS-card (or install a faster GAL).
- When the PAK is used with a MegaSTE make sure to set the processor clock to 8MHz and turn off the board cache (remember to save the settings) otherwise the PAK will not work.

- You must ensure that the power supply is not overloaded if you operate the PAK in conjunction with other extensions. The original power supply is generally not very strong.
- It is important to provide solid ground connections (short and thick). The PAK provides several connection points for this on the board (GND). Also a direct power connection to the +5V pad on the PAK is not a bad idea.
- IDE adapters can cause problems in principle so it may be better to use SCSI.
- Unfortunately, some graphics adapters can cause problems. Candidates for this are the NOVA adapters, the VOFA and the Multiboard. More on this later.

### 1.4 Features of the PAK68/3-030

- 68030 processor, 32-bit instruction and data cache on-chip, PMMU
- 68881/882 FPU (optional)
- 32KB second level cache (optional)
- 32-50 MHz clock frequency
- EPROMs with a custom TOS 3.06 on the PAK (optional)
- Switchover mode to operate with a 68000 CPU (optional)
- High compatibility with Atari mainboards and other hardware through a clean bus interface (the PAK even runs on 68000-based Macintosh systems!)

## 2. Building the PAK68/3

### 2.1 Prerequisites

This chapter isn't relevant to owners of the finished device. If this applies please continue reading from Chapter 3 onwards.

We assume that the empty board has been purchased by persons who know what they are doing and can get the components themselves. Those who have purchased the (partial) parts kit still need the remaining components. These should be available at any well-stocked local electronics store.

A good electronics soldering iron (regulated, max. 25W) and a good desoldering pump should be on-hand. Also, if necessary, some desoldering braid. Of course you will need flux-cored electronics solder and a fine side-cutter. If any step in the process seems too daunting then just ask a friend with some experience for help or take advantage of our installation service if all else fails.

If you want to build the PAK yourself then please take great care in the construction since the board is a 4x multilayer PCB and errors may be difficult to find after-the-fact and can be costly.

## 2.2 Clock Buffering - Part 1

Before you start building you will need to decide in principle if you want to use clock buffering or not. This is because additional components are required for buffering as well as some standard components being changed. So you can save time with a little extra effort and consideration. Though you can always retrofit or remove the clock buffering later, it's just extra work that can be avoided.

To help you make the decision here is an overview of the possibilities:

- **No Clock Buffering**

  This really only makes sense if you intend to install a FRAK/? in the near future since the clock buffering is built-in and so it is not used on the PAK even if it is installed! Otherwise you can only do without buffering on a 32 MHz PAK and cannot use a FPU.

  So now if you have decided against clock buffering then you should close the bridge between R47 and the quartz oscillator with some solder immediately so you do not forget; otherwise the PAK will not run since clearly there will be no clock.

- **Clock Buffering - Permanently Soldered**

  If you will use the PAK long-term without equipping a FRAK/? Then we generally recommend clock buffering for the PAK above 32MHz and always with a FPU (at 50MHz it is

pretty much mandatory!). So you will need to obtain the additional/other components for the clock buffering and equip the PAK accordingly during construction.

Attention! With FRAK/? the clock buffering must not be used!

- **Clock-Buffering - Variable**

  If you intend to play around with the clock buffering (tests with/without FRAK/?, fiddling with the clock frequency, etc.), you should consider whether or not to use solder cups for the analog components of the clock buffering to make it easier to replace those components at a later time. The same applies to R41 and R43 if you intend to experiment with the board clock.

  Attention! With FRAK/? the clock buffering must not be used!

## 2.3 The Construction

Regarding the order of construction we recommend first placing the flat components i.e. all the analog components such as resisitors, capacitors and the resistor network. Then solder the 74F86, the four cache SRAMs and the 16V8-GAL P3-PUK-A directly to the board (without socket). Now place the IC sockets and the IC plug adapter pins; (using a 64-pin socket below these can serve as a positioning aid). The board-edge pads of the two 64-pin SIL rows are for one socket of the PAK (U7, i.e. for a 68000) and the board-center pads are for the IC adapter pins for plugging into the mainboard socket (CON2). By the way, it is best to place the IC adapter pins on the PAK first then the SIL strips. Now all that remains are the jumper pin headers and the semiconductor ICs which will be placed into their sockets just before installation. The jumpers are explained in more detail in Chapter 4.2.

If you have decided to buffer the clock, solder the 74F00 on the solder side without a socket. Pin 1 has a square pad. For R47 use 10 ohms instead of 33 ohms. For R48 use 68 ohms and for C43 use 220pF (between GAL sockets) Also, in this case, the solder bridge between R47 and the oscillator on the bottom must remain open.

Attention! With a FRAK/? the clock buffering must not be used!

The PAK should now be soldered except for any possible wires or cabling. We are moving closer to the installation in Chapter 3.

# 3. Installing the PAK68/3

## 3.1 Preparing the Mainboard

To start with: The ideal target system for a PAK is a MegaST. With the 520ST and 1040ST(F) there are sometimes problems due to the older board design (keyword: bus terminations) and the power supply. With the 1040STE and MegaSTE the PLCC CPU can be a stumbling block since most PLCC-to-DIP adapters are apt to be problematic.

The important thing is that the CPU must be socketed for the installation of the PAK since it is placed in leiu of the original CPU. However, with the switchover GAL P3 on the PAK, a 68000 can be used as a fallback alternative. With this being said, if your CPU is not socketed now is the time to do it. The best way to do this is to use a fine side-cutter and snip the CPU pins close to the mainboard. This renders the CPU unusable, but a new CPU costs just 10,- DM. A new mainboard would be much more expensive if you were to require one. After snipping the pins, you can simply hold each pin remaining in the mainboard with some tweezers and easily unsolder them. Then clean the holes with a desoldering pump. (tip: heat from the component side and suction from the solder side!) and finally clear the board of any solder blobs or solder splashes remaining from the desoldering process. Now you are just missing the DIP precision socket. Please pay attention to the correct alignment of the socket in relation to the mainboard stenciling. If there was a small board present on the CPU (only MegaST and you can just get rid of it with the CPU) you have to close the cut trace made by Atari on the solder side of the mainboard. To do this, run one wire from pin 12 of the CPU socket to pin 12 of the Megabus connector on the bottom of the board.

Using a new CPU to functionally test the new socket wll ensure the conversion was successfully completed.

If you intend to convert a 1040STE or MegaSTE for the PAK then you must first remove the CPU from its socket, install a PLCC-to-DIP adapter then get a 68000 CPU in DIP form to test it with. But you should be clear that we warn against contact problems when using a PLCC-to-DIP adapter.

For trouble-free operation of the PAK we strongly recommend removal of the blitter if it is installed (i.e. MegaST). The reason is a bus transfer protocol error that can lead to crashes or DMA issues (which is the reason for the small add-on board in some MegaSTs). Apart from that, using the blitter in concert with a PAK will incur a speed penalty: The blitter is a DMA device so with every blitter activity the second level cache of the PAK is cleared which effectively slows things down. Regarding working speeds, the PAK outperforms the blitter anyway from 32MHz onwards. So if you do decide to remove the blitter, please do not forget the two solder bridges, so the computer doesn't hang the next time you turn it on.

So that there are no problems with the mainboard RAM, it should have a max access time of 100ns. Unfortunately there are configurations with 120ns or even 150ns. If that is the case there will certainly be problems. If you are unlucky enough to have such a computer then you must first ensure you have fast enough mainboard RAM. Depending on the mainboard, this can grow into quite a soldering job. Unforunately this is a broad topic and goes beyond the scope of this manual. If you can't ensure the mainboard has fast enough RAM then we advise against installing the PAK. If necessary, an experienced friend may be able to help you. Unfortunately we cannot offer this service since the procedure is far too expensive for anyone to want to pay... However, it is important to note that for the installation of a memory expansion if you take the power supply from the vicinity of the RAM on the mainboard then you should bridge the built-in Atari choke which seperates the RAM-Vcc section of the mainboard from the rest.

This choke is a noise filter, but this only works if the choke is not loaded too heavily. Otherwise the resistive part of the component will predominate and the supply voltage (compared to the remaining potential) will drop. And again as a general point, the GND connections should always be short and thick.

Please make sure that you do not overtax the power supply! If you want to use a memory expansion, a graphics card and the PAK then a stronger power supply will be required (at least 50W). If in doubt, measure the supply voltages at various points in the computer. Deviations of more than 2.5% are outside of tolerance.

For the 520ST and 1040ST check the bus terminations to be on the safe side. In older revisions the pull-ups for the data and address busses are 10k ohm. If you know how and where to change them, we recommend 4.7k ohm for the data bus and 3.3k ohm for the address bus.

When you are modifying and testing the computer the clacking sound will get on your nerves if you have forgotten to connect the keyboard (popular case with MegaST). Here is a tip on how to change that. The problem is that Atari has placed a pull-down resistor on boards up to and including the MegaST at the keyboard ACIA's receiving line (from the TT onwards they have changed this). This causes a constant null character reception and results in the annoying clacking sound. All you have to do to stop this nuisance is to convert the pull-down to a pull-up resistance. For this, follow the lead from the keyboard ACIA pin 2. From the chip it goes to a 10k resistor and the choke, which then leads to the keyboard jack. The 10k resistor goes to ground on the other side. Disconnect that side from the mainboard and connect it to +5V.

## 3.2 Preparing the PAK

We recommend a direct power supply connection to the PAK through the large pads found under the 68000 socket. If you do this, it is best to use a 5.25" floppy power plug Y-cable where you would disconnect the plug from one of the branches (disconnect the 12V wire, usually yellow, all the way back to the source) so that you have the +5V wire (usually red) and the two GND wires (usually black) to connect to the pads. Additionally we recommend connecting two wires (short and thick) from the two GND pads next to the 68000 socket to GND points on the mainboard, but taken as close as possible to the 68000 socket. To keep these connections separable, it is best to use 6mm flat connectors (keyword: "auto"). Snip off the flat pin of the plug and solder directly to the mainboard ground. Solder the jack to the cable going to the PAK.

Next you should jumper the PAK according to your configuration. The jumper assignments can be found in Chapter 4.2. A tip in this context: If you have a FRAK/? and want to easily access J4 (SLC) or J5 (PAK-Enable) (because the FRAK/? sits above the PAK and therefore there is no access to put/remove the jumpers) you should extend the jumper with an additional 2-pin post and some wiring on the solder side. Then fix it to the edge of the board with, for example, hot glue. This makes the jumper easily accessible from the edge of the board even if a FRAK/? is installed above the PAK. Even though the post pins on the PAK itself have become useless for configuration, the GND pin is used in the FRAK/? patch anyway and would have made the use of the jumper impossible.

If you are building the PAK yourself then now is the time to put in the remaining semiconductor components. Please pay attention to the correct polarity (alignment) of the components. Pin 1 of an IC is always inserted in the direction of the notch in the socket or sometimes pin 1 has a square pad. For the CPU and FPU, pin 1 is usually indicated by a golden mark on the top (always on a corner). When inserting the GALs, please follow the instructions in Chapter 4.1.

## 3.3 Installing the PAK

Now you can put the PAK in the mainboard socket. Please make sure that you have the necessary socket height so that the solder side of the PAK does not come in contact with components on the mainboard; that would create the risk of a short-circuit! Another tip in this context: If you intend to remove and install the PAK often, then install an additional socket to extend the plug-in cycles for the mainboard socket (since you would be engaging the additional socket and the mainboard socket will stay "fresh" longer).

For the initial tests you should have as few peripherals connected as possible. In particular, the hard drive should be disconnected for safety reasons! Please do not forget the power supply and GND cables if you decide to use them (which we recommend). This sets us up for a first test of the PAK.

## 3.4 Initial Testing

Turn on the power supply. There should be an Atari logo in the upper left corner of the screen. If there is still no Atari logo after 10 seconds, switch off the power supply to avoid damaging any components in case there are any problems with the construction of the PAK. If the screen remains completely black then immediately turn off the power supply and check if any components have become very hot! If this is the case, there is usually a problem with reversed polarity (Vcc and GND swapped, an IC the wrong way in a socket, etc.) or some other serious construction or configuration error. More in Chapter 5.

If the PAK is functioning properly then shortly after the logo the memory test will begin which you should run through the first time for safety's sake. Later this memory test can be easily skipped by pressing the space bar to cancel it. After this the desktop should appear. Now you can, for example, test the system speed with the benchmark programs on the included floppy disk.

If the PAK won't run right away it doesn't necessarily mean there is a hardware fault. In this case, see Chapter 5 for a checklist.

Now it is time to perform an initial test with the hard drive. Again, for safety reasons, please test only with unimportant data especially when performing write operations! Also, keep in mind that the hard disk driver can cause issues if it is an older version. We recommend using the latest version of HDDriver from Uwe Seimet.

# 4. Configuring the PAK68/3

## 4.1 The GAL Set

The flow control of the PAK is performed by five 20v8 GALs. So the "intelligence" of the PAK is contained in these programmable logic devices and can be replaced or updated to newer versions. Generally, if your GAL equations are not up-to-date we recommend updating to the most current versions of the PAK GALs. If you cannot program GALs yourself, you can obtain programmed GAL sets from us. The JEDEC files of the current GAL equations for our projects can be found on our website (www.wrsonline.de) or on the inlcuded disk in the file WRSGAL??.LZH.

At the time of printing, the following GALs are up-to-date for the PAK:

| | | |
|---|---|---|
| **U1** | P13-50d | |
| **U2** | P2-ST | |
| **U4** | V4-50ac | |
| **U5** | V5-51a | |
| **U6** | P6-ST | without FRAK/? |
| | P6-F05 | with FRAK/? (Disconnect Pin2/CON1!) |
| **U3** | P3-PUK | (16v8, old PAK layout with wiring) |
| | P3-PUK-A | (16v8, new PAK layout) |

Explanation: Un specifies the position on the board, P* stands for a public standard GAL and V* for a GAL which is still a beta release. As you can see, two GALs are not quite public standard yet, but candidates for it. We will release a new GAL set shortly.

For P3, in contrast with the others, a 16v8 GAL (15ns) is required which, incidentally, can be soldered directly to the board to provide additional clearance.

## 4.2 The Jumpers

| Jn | Name | Funktion |
|---|---|---|
| J1 | MMU-Disable | **open=enabled** |
| J2 | CPU-Cache disable | **open=enabled** |
| J3 | FPU-Enable | **open=disabled or not available** |
| J4 | SLC-Disable | **open=SecondLevelCache enabled** |
| J5 | PAK-Enable | **closed=enabled** |
| J6 | BR | **closed,** but only if the P3-PUK GAL is not wired! With P3-PUK-GAL open (unequipped) |
| J7 | ROM | **1-2=ROM on the PAK active**<br>2-3=inactive or not available |
| J8 | ROM_CS | **1-2=/ROMCS to GND for faster access**<br>2-3=/ROMCS connected to /ROMOE |
| J9 | CPUCLK | **1-2=asynchronous clock, i.e. from FRAK**<br>2-3=synchronous 16MHz clock (NOT with FRAK!) |
| J10 | FPUCLK | **1-2=asynchronous clock like CPU**<br>2-3=synchronous 16MHz clock (the FPU should not run slower than the CPU) |
| J11 | Cache-Control | **1-2=via MMU**<br>2-3=reserved, not used open=SLC always on |

Remarks:
**Standard** in this Notation
Pin 1 on 3-pin jumpers has a square pad
enabled = activated, disabled = deactivated

## 4.3 The TOS

The PAK is a pretty large change for a ST(E) system. Specifically the 68030 processor since normally there is only one 68000 installed. In order to support this processor correctly (PMMU, VBR, extended stack frames, cache-on-chip, etc.) a suitably modified TOS is required. And in order to increase the speed of this PAK-TOS it is placed directly on the PAK in EPROMs. This way the CPU can read the data with the full bus width of 32-bits which is considerably faster than reading it via the mainboard.

Atari has already released a 68030 optimized TOS for the TT; TOS 3.06. However, since the TT differs significantly from the PAK hardware, a few changes (patches) had to be made so that this TT-TOS would work on the PAK. So began PAK-TOS, a patched version of TOS 3.06 used on the TT.

Unfortunately, due to licensing reasons, we cannot offer a ready-made version of this PAK-TOS as TOS is still under the copyright of Atari (or whatever is left of it). So we offer the program TOS-Patch with which you can see the changes to the TOS versions regardless of the TOS binary file itself. Anyone can use TOS-Patch with an appropriate patch file (containing a list of necessary changes) to create their own TOS.IMG file to burn a PAK-TOS for their PAK. This image file is burned into four megabit EPROMs (27C1001-120ns) and plugged into the PAK. The current patch file for PAK-TOS will be available shortly on our website (www.wrsonline.de). If you need help in this regard, please contact us directly.

The following country-specific adaptations of PAK-TOS are currently available:

- German (GER)
- American (USA)
- English (UK)
- French (FRA)

For all but the German version of PAK-TOS, boot roms on the mainboard are necessary. These must contain the address of the PAK-TOS ($FEE00000) as the start PC in the second 4 bytes (usually the address $00FC0000). The German version of PAK-TOS does not need any boot roms (but there must be some roms on the mainboard) because a trick is used when reading the TOS start address. Unfortunately this has not yet been tested sufficiently in the "heart and soul" of the other country-specific versions.

You can find the assignments for the PAK ROM slots in Appendix C.

For the sake of completeness it should be mentioned that theoretically the PAK also works with TOS 2.06, but only with restrictions. So we strongly advise against using TOS 2.06:

- Fast RAM cannot be used
- Virtual memory is not possible
- Some older hard disk drivers will not work properly
- Memory protection is not possible

## 4.4 Clock-Buffering - Part 2

The 68030 processor is very sensitive as far as the quality of the clock signal is concerned. If the clock is not "clean" there can be relatively bad consequences. With crashes caused by a "dirty" clock, DMA problems and problems accessing the mainboard have been observed. In the most extreme cases the computer didn't even boot anymore.

The higher the clock rate, the harder it is to keep the clock signal clean. An adequate clock is achieved by a reasonable termination of the clock line. However, this is predicated on the requirement of sufficient driving force for the clock source. Unfortunately, whether in a metal or plastic housing, the quartz oscillators are a little underpowered. Since in the planning phase the PAK was originally designed for 32MHz operation, the first version of the PAK was not designed with optional clock buffering and termination (the 50MHz speed madness came later. Also FPUs were expensive and very rare at that time).

This has, however, changed with the second edition of the PAK board (A layout) as appropriate components are provided in the layout.

The clock buffering therefore always consists of a buffer or amplifier circuit of the clock signal source and the termination of the clock line on the PAK. Furthermore, the presence and version of a FRAK/? plays a role since on the FRAK/? the clock buffering is already done. But in any case the clock line on the PAK has to be terminated. An overview:

- **WITHOUT FRAK/?**
  - **without clock buffering (max. 32MHZ, no FPU)** Close the bridge between R47 and the quartz oscillator with some solder
  - **with clock buffering (from 32MHz and/or with FPU)** Leave solder bridge between R47 and quartz oscillator open; place a 74F00 on the solder side (!) under the quartz oscillator U23; R47=10 ohm (instead of 33 ohm); series circuit of 68 ohm resistor and 220pF capacitor from U1 Pin 1 to U5 Pin 12; alternatively use R48=68 ohm, C43=220pF (A-Layout)
- **WITH FRAK/1**
  - Termination of the clock line on the PAK series circuit of 68 ohm resistor and 220pF capacitor from U1 Pin 1 to U5 Pin 12; alternatively use R48=68 ohm, C43=220pF (A-Layout)
- **WITH FRAK/2**
  - Termination of the clock line on the PAK 100 ohm resistor from U1 Pin 1 to U5 Pin 12

The above values of the analog components are standard values. It may be necessary to adjust them slightly, but this is only possible with relatively serious measuring equipment (at least 100MHz oscilloscope) and quite a lot of expertise. However, an adjustment should be so rare that we do not want to get into the details here.

## 4.5 PAK and 68000: Alternate Operating Mode

For compatibility purposes it is possible to alternatively operate a 68000 processor on an existing PAK. However, it can not be switched over during operation. A cold start is necessary to remove the invalid system variables. The switchover takes place via jumper J5 and you can easily connect a (not too long) cable and toggle switch to it.

To be able to use this fallback mechanism, a 68000 CPU must of course be plugged into the socket (U7) on the PAK that is provided for this purpose. Furthermore, J6, which is for PAK-only use, must be left open. Last but not least, the switchover GAL P3 has to be equipped and depends on the board version.

Owners of the new A-layout must use version P3-PUK-A. The GAL can be soldered directly as the equations will probably never change. This completes all modifications.

Owners of the older PAK layout have to use version P3-PUK and unfortunately re-wire 8 lines by hand.:

1. /BG_68K Pin 11 U7 to Pin 9 PUK-GAL
2. /BR_68K Pin 13 U7 to Pin 13 PUK-GAL
3. E_68K Pin 20 U7 to Pin 6 PUK-GAL
4. /BG_PAK Pin 11 CON2 to Pin 12 PUK-GAL
5. /BR_PAK Pin 13 CON2 to Pin 8 PUK-GAL
6. E_PAK Pin 20 CON2 to Pin 15 PUK-GAL
7. /PAK_EN Pin 2 J5 to Pin 2 PUK-GAL
8. /BR_20 Pin 1 J6 to Pin 19 PUK-GAL

## 4.6 PAK with Mainboard Clock Greater Than 8MHz

The PAK is designed for use with an 8MHz bus system. However, there is nothing against using a higher bus clock if you make the necessary changes for it. In particular this is the clock doubler circuit whose RC elements are "calibrated" to 8MHz. Depending on the board clock you have to resize R41 and R43 so that the clock halves are again about the same size. Unfortunately, this sounds easier than it is in practice and it requires at least a 100MHz oscilloscope to observe the double mainboard clock with sufficient accuracy.

As a guidleine for 12MHz bus clock: R41=430 ohms, R43=330 ohms.

In addition it may be necessary to lower the bus terminations of the mainboard. Again as a guide, 4.7k for the data lines and 3.3k for the address lines.

Sometimes it is even necessary to replace the mainboard RAM data bus drivers. From experience we can say that at an 8MHz board clock HCT-types are best for the two 74LS244 and for the two 74LS373 the F-types are best. At 12MHz F-types should be used for all drivers.

Attention! Please do not use ACT-types! While these are very fast, they do more damage to the waveform with too much drive power than their speed can ever make up for.

### 4.7 PAK and PuPla/?

We should briefly mention a very important extension to the PAK here; the buffer board PuPla. Now available in the second version (PuPla/2), this extension is an important tool to solve a variety of mainboard related issues. The PuPla/2 even helps with frequent FPU errors. The essential function of the buffer board is to disconnect the PAK bus from the mainboard bus so that the slow mainboard cannot disturb the PAK on local bus cycles after a mainboard bus cycle. Additionally the PuPla/2 relieves the CPU significantly on the address and data lines. It has an especially postive effect with a FRAK/? because the CPU is already warm enough. More information can be found at our website (www.wrsonline.de) or directly from us.

## 5. Troubleshooting

The PAK is not a real plug&play system. Unfortunately some things have to be optimized or retrofitted by hand.

On the other hand, the PAK offers a hefty speed increase and operational stability once it is properly set up. The following is a "first aid" in troubleshooting. As far as possible the tips are in the form of checklists.

## 5.1 Startup Problems

**After powering on the PAK does not start at all and the screen remains dark.**

- Is the PAK correct in the mainboard socket? Possibly plugged-in off by a row of pins?
- All components where they belong? Oriented correctly? Check QO, GALs, drivers, ROMs.
- J5 set?
- Without clock buffering: Solder bridge closed?
- An additional pull-up resistor may be required on the reset line as it tends to oscillate, especially at higher clock speeds. Solder a 1k ohm resistor from CON2 Pin 18 to CON2 Pin 14, preferably on the component side of the PAK. Alternatively: 1k SMD resistor and wire pieces from Vcc pin of the F86 to CON2 Pin 18 on the solder side of the PAK.
- With FRAK/?: F541 driver on it? Power connected?
- For any TOS versions other than GER (Germany) boot ROMs are required!

**When I turn on the PAK, it seems to reset constantly, just after a picture appears.**

- 1k reset pull-up (see above)
- Clock line terminated correctly?
- Check TOS on the PAK and on the mainboard

## 5.2 Stability Problems

There are three main reasons for stability problems:

1. Contact Problems

These can often occur when you frequently insert and remove the PAK. For this nothing much helps other than to completely replace the relevant socket.

2. Clock Quality
   If the clock signal is not clean enough, the 68030 can be a big problem. See Chapter 4.4.
3. Mainboard Problems
   Here again there are several possibilities:
   - The mainboard RAM is too slow. For the mainboard the maximum is 100ns, 80ns is better and 60ns is optimal. The RAM really can't be fast enough, especially if used together with a PuPla/2!
   - The bus load is too high. In this case a PuPla/2 can help.
   - The mainboard bus termination has too much slack. Recommendation: 4.7k for the data lines and 3.3k for the address lines.

Additionally there can be problems when overclocking chips. Classic example is a 33MHz CPU operating at 40MHz. In the long run cooling doesn't really help; just don't overclock! The manufacturer has their reasons if there is a maximum clock on a component...

If a FRAK/? is in operation there may be problems if the RAM (on the FRAK/?) is not fast enough for the clock frequency used on the PAK. See the FRAK/? manual. Sometimes there may be problems with the burst mode. Just turn off the burst mode for a test.

At 50MHz clock frequency you should also try using a 10ns GAL for PAK.U1 and FRAK/2.FR9.

## 5.3 DMA/Floppy Problems

Unfortunately some older hard disk drivers are not updated for the PAK. We therefore recommend the latest version of HDDriver by Uwe Seimet. This disk driver is constantly updated and maintained so that makes it a good solution.

Another reason for DMA problems (hard disk/floppy problems) can be an inaccurate clock. Most of the time these problems are related to two bombs on hard disk accesses. See Chapter 4.4. DMA problems have also been observed in non-current

GAL sets or in non-recommended/incorrect GAL configurations. Please always use the current GAL set!

In some computers an improvement has been acheived by buffering the ACSI signals of the DMA chip. We offer a corresponding buffer board. This solution is only applicable to computers without a buffered DMA chip, i.e. 520ST, 1040ST and MegaST. The "E"-series computers already have this buffering. But the buffering of the DMA chip isn't a guaranteed fix as this method helps only in the rarest of cases.

Also sometimes, often in connection with a PuPla/2, a floppy problem occurs which can be described as follows: disk access becomes very slow, directory contents and small files can usually still be read, but large files cannot ("Data on the disk in drive A: may be damaged", "Drive A: is not responding"). Writing works very rarely or not at all ("The disk in drive A: is physically write-protected", which wasn´t actually true). If you switch off all caches (CPU internal and SLC) disk accesses are almost normal. These problems can be attributed to incorrect handling of the DMA chip (which Atari does wrong in TOS itself, unlike Atari's own recommendation...). In most cases, patching the operating system fixes these errors. The current version of PAK-TOS (G3) aready has this patch leaving only MagiC users still affected. The byte sequence $3CBC0180 should only appear three times in the MagiC operating system file (MAGIC.RAM). The first occurance of this byte sequence should under no circumstances be changed! The second and third occurences should be changed to $3CBC0080. This should eliminate the problems, but in any event things should not be worse than before.

## 5.4 Additional Extensions

Some additional extensions or add-ons may cause problems when used in concert with a PAK. The problem usually lies with the extension itself and not the PAK. Most extensions expect the bus timing to be set for a normal 8MHz 68000 system and cannot handle the much faster PAK.

In this context we would like to point out that extensions that adhere to correct 68000 timings usually have no problems with the PAK because the PAK strives to be as accurate as possible with precise timing! But if you do not match the timing exactly with your developments, which may not even be noticeable on an 8MHz 68000, it can lead to dire results on the (much faster) PAK. Just one example: An 8MHz 68000 cannot access the mainboard on two consecutive bus cycles, but a PAK can nicely!

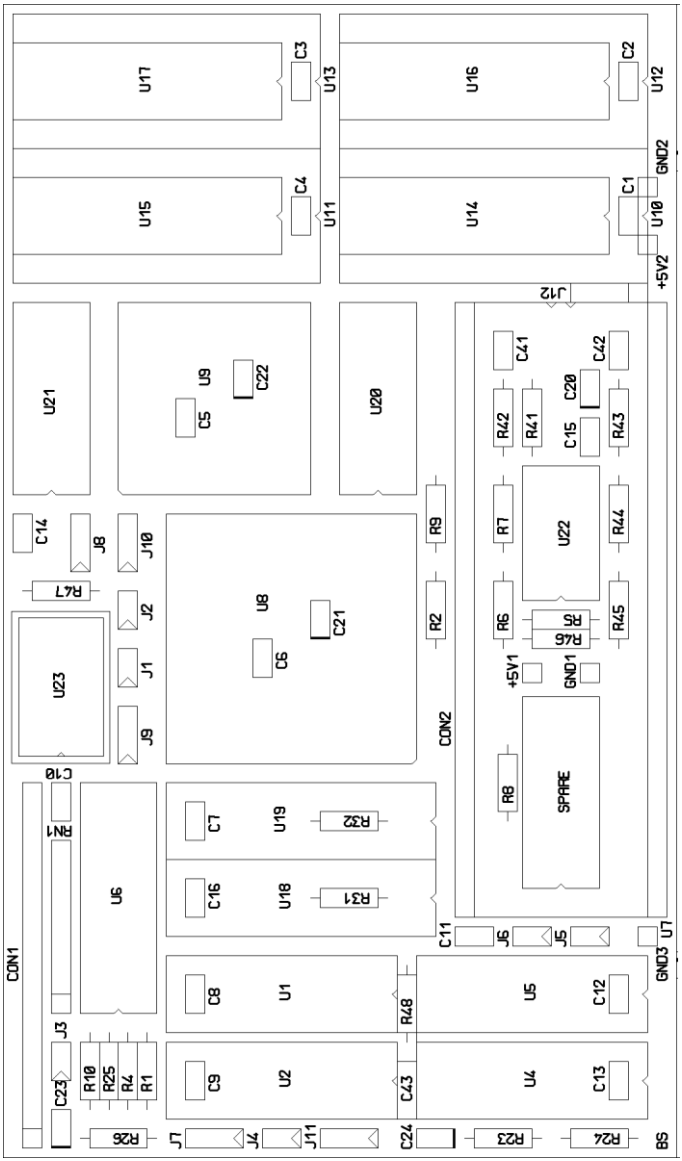
A TOS extension using a GAL that is too slow can lead to problems with mainboard access. The TOS card should use a GAL with a maximum speed of 15ns ("-15" on the chip), but sadly there are some with 25ns GALs. In that case, your only recourse is to remove the extension or get a faster GAL from the manufacturer.

Some IDE adapters can also cause problems, usually due to poor timing of GALs that are too slow. Unfortunately, nothing can help with these extensions other than removing them and choosing instead the better SCSI system.

Some graphics adapters may cause problems with the PAK. Again, in the end the solution is usually to choose a different graphics adapter...

If problems occur using the PAK with additional extensions installed and these problems cannot be observed without the PAK then there is no other choice but to completely remove all other exetensions (i.e. to restore the computer to its original state) and then install them again one by one with the PAK. This should reveal which extension is causing the problem. Exceptions to this are extensions that do not depend on the bus system so, for example, a HD module or a serial interface upgrade shouldn't have any impact.

# Appendix A – Component Layout



## Appendix B – Parts List

| Position | Qty | Description |
|---|---|---|
| U1,2,4,5,6 | 5 | GAL20v8, 15ns, appropriately programmed |
| U3 (SPARE) | 1 | GAL16v8, 15ns, appropriately programmed for 68000 switch-over |
| U8 | 1 | MC68030 (CPU) |
| U9 | 1 | MC68882 (FPU) |
| U10-U13 | 4 | 270010, 120ns, appropriately programmed (ROM) |
| U14-U17 | 4 | (Cache-)SRAM, 20ns, 8Kx8 (e.g. TC5588) |
| U18, U19 | 2 | Tag-RAM, 20ns (e.g. ST-MK48S74) |
| U20, U21 | 2 | 74F541 |
| U22 | 1 | 74F86 |
| U23 | 1 | Quartz Oscillator 32-50MHz |
| RN1 | 1 | Resistor Network 4.7k ohm x8 Array |
| R1, R4, R7, R10, R23-R26 | 8 | Resistor 4.7k |
| R2, R5, R6 | 3 | Resistor 1k |
| R8 | 1 | Resistor 2.2k |
| R31, R32 | 2 | Resistor 330 ohm |
| R41, R43 | 2 | Resistor 560 ohm |
| R42 | 1 | Resistor 10k |
| R44-R47 | 4 | Resistor 33 ohm |
| C1-C16 | 16 | Ceramic Capacitor 100nF, 2.54mm |
| C20-C24 | 5 | Tantalum Capacitor 10uF/16V, 2.54mm |
| C41, C42 | 2 | Ceramic Capacitor 22pF, 2.54mm |
| J1-J6 | 6 | Pin Header, 2pin |
| J711 1 | 5 | Pin Header, 3pin |
| CON1 | 1 | SIL Socket 19pin |
| CON2 | 2 | SIL Plug-In Adapter 32pin (mainboard) Attention! CON2 are the "inner" pads |
| ST1 (U7) | 2 | SIL Socket 32pin (68000 socket) Attention! ST1 are the "outer" pads |

Changes to the new A version of the PAK layout.

- new resistor R9: 33 ohms. Be sure to equip!
- two additional ground points and a Vcc pad on the edge of the board next to the 68000 socket
- new jumper J12; for test purposes only (Flash-ROM). Do not populate
- the PUK-GAL (U3) is already fully wired, but with a different pin configuration (P3-PUK-A)
- optional clock buffering, see Chapter 4.4

## Appendix C – TOS ROM Table

Byte assignment for a TOS longword:

| **Bit** | **TT** | **PAK68/3** | **PAK68/2** | **WRS** |
|---|---|---|---|---|
| D24 - D31 | EE | U10 | U11 | HIH |
| D16 - D23 | OE | U11 | U10 | HIL |
| D8 - D15 | EO | U12 | U9 | LOH |
| D0 - D7 | OO | U13 | U8 | LOL |