256K X 8 Bit CMOS Video RAM

FEATURES

- **Dual port Architecture**
  256K x 8 bits RAM port
  512 x 8 bits SAM port
- **Performance range :**

Parameter \ Speed	-6	-7	-8
RAM access time (t_{RAC})	60ns	70ns	80ns
RAM access time (t_{CAC})	15ns	20ns	20ns
RAM cycle time (t_{RC})	110ns	130ns	150ns
RAM page mode cycle (t_{PC})	30ns	35ns	40ns
SAM access time (t_{SCA})	15ns	17ns	20ns
SAM cycle time (t_{SCC})	18ns	22ns	25ns
RAM active current	110mA	100mA	90mA
SAM active current	55mA	50mA	45mA

- **Fast Page Mode with Extended Data Out**
- **RAM Read, Write, Read-Modify-Write**
- **Serial Read (SR) and Serial Write (SW)**
- **Read / Real time read transfer (RT, RRT)**
- **Split Read Transfer with Stop Operation (SRT)**
- **Write and Split Write Transfer with Stop Register (New and Old Mask), (WT,SWT)**
- **Nibble Write Operation**
- **Block Write (BW) Flash Write (FLW) and Write-per-Bit with Masking Operation (New and Old Mask)**
- **$\overline{CAS}$-before-$\overline{RAS}$, $\overline{RAS}$-only and Hidden Refresh**
- **Common Data I/O Using three state RAM Output control**
- **All Inputs and Outputs TTL Compatible**
- **Refresh: 512 Cycle/8ms**
- **Single +5V± 10% Supply Voltage**
- **Plastic 40-Pin 400mil SOJ**
- **Plastic 40/44-Pin 400mil TSOP II (and Reverse Type)**

GENERAL DESCRIPTION

The Samsung KM428C258 is a CMOS 256K x 8 bit Dual Port DRAM. It consists of a 256K x 8 dynamic random access memory (RAM) port and 512 x 8 static serial access memory (SAM) port. The RAM and SAM ports operate asynchronously except during data transfer between the ports.

The RAM array consists of 512 bit rows of 4096 bits. It operates like a conventional 256K x 8 CMOS DRAM. The RAM port has a write per bit mask capability. Data may be written with New and Old Mask. The RAM port has a Fast Page mode access with Extended Data out, Block Write and Flash Write capability. Nibble write control can be applied in write, Block Write, Flash Write, Load Mask Register and Load Color Register cycles.

The SAM port consists of eight 512 bit high speed shift registers that are connected to the RAM array through a 4096 bit data transfer gate. The SAM port has serial read and write capabilities.

Data may be internally transferred bi-directionally between the RAM and SAM ports using read, write and programmable (Stop Register) Split Transfers.

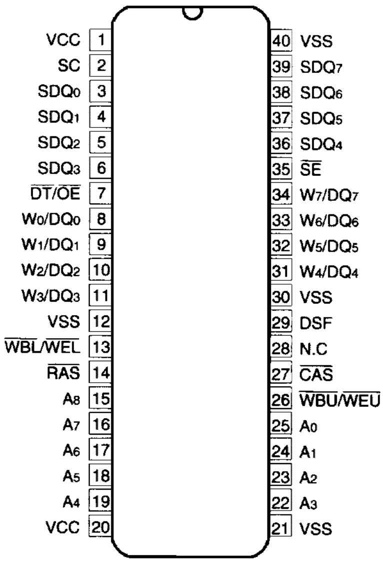
Refresh is accomplished by familiar DRAM refresh modes. The KM428CV258 supports $\overline{RAS}$-only, Hidden, and $\overline{CAS}$-before-$\overline{RAS}$ refresh for the RAM port. The SAM port does not require refresh.

All inputs and I/O's are TTL level compatible. All address lines and Data Inputs are latched on chip to simplify system design. The outputs are unlatched to allow greater system flexibility.

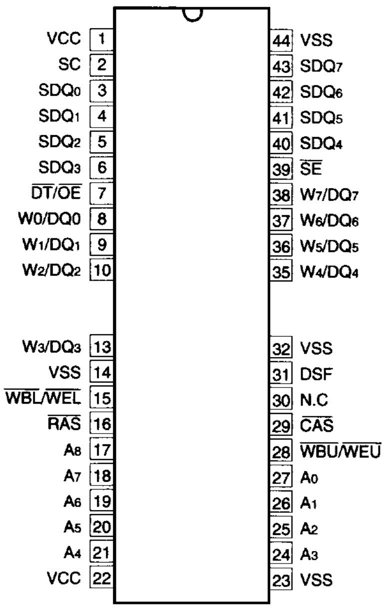
Pin Name	Pin Function
SC	Serial Clock
SDQ_0-SDQ_7	Serial Data Input / Output
$\overline{DT}/\overline{OE}$	Data Transfer / Output Enable
$\overline{WBL}/\overline{WEL}$,	Write Per Bit / Write Enable
$\overline{WBU}/\overline{WEU}$	(Lower/Upper)
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
W_0/DQ_0-W_7/DQ_7	Data Write Mask / Input / Output
$\overline{SE}$	Serial Enable
A_0-A_8	Address Inputs
DSF	Special Function Control
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C	No Connection

PIN CONFIGURATION (TOP VIEWS)

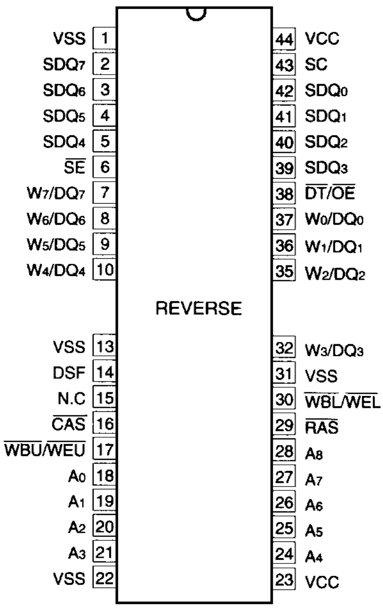
40 Pin 400 mil SOJ



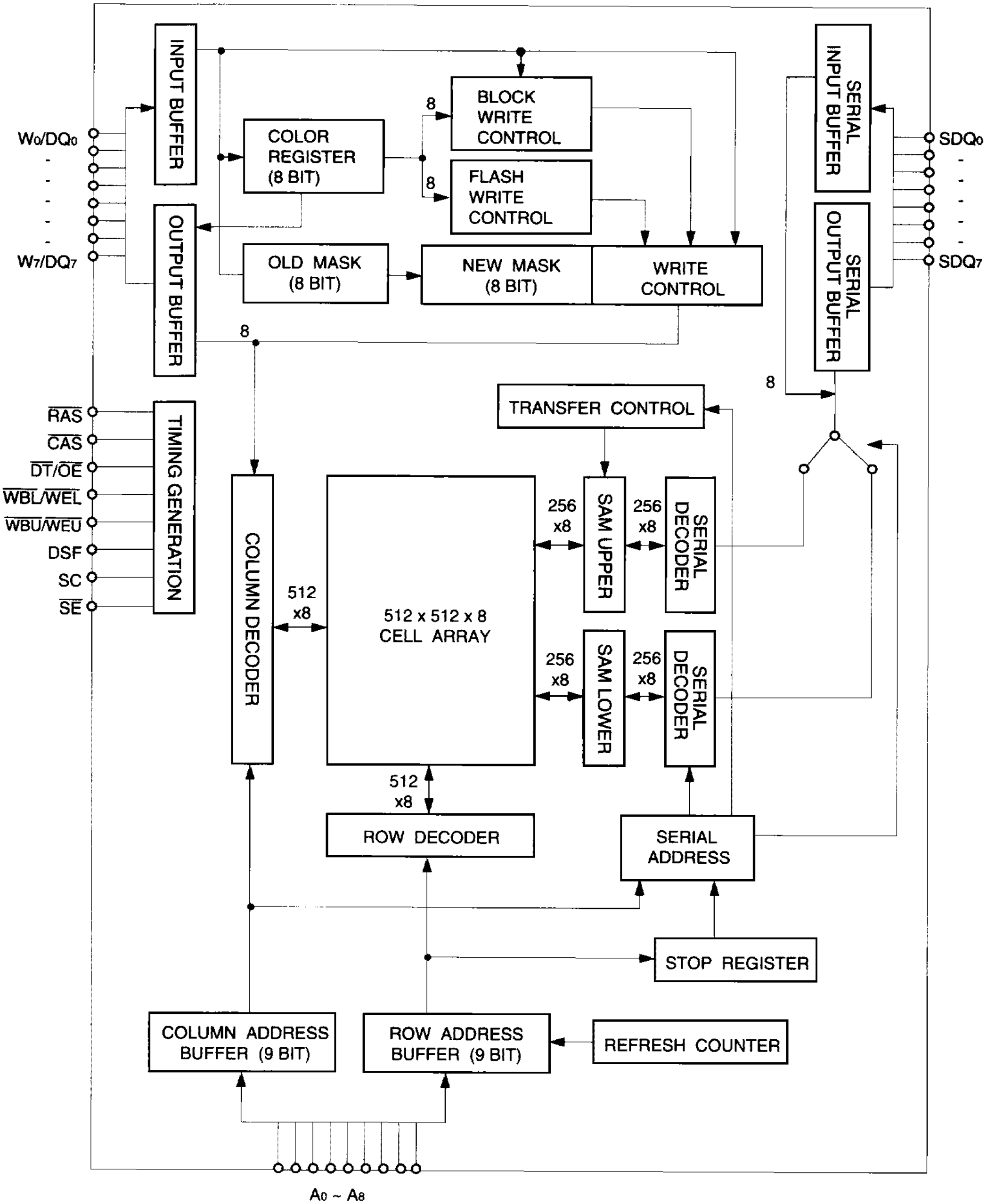
40/44 Pin 400 mil TSOP II



40/44 Pin 400 mil TSOP II



BLOCK DIAGRAM



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FUNCTION TRUTH TABLE

Mnemonic Code	$\overline{RAS}$				$\overline{CAS}$	Address		DQi Input		Write Mask	Register		Function
	$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WE}$	DSF	DSF	$\overline{RAS}$	$\overline{CAS}$	$\overline{RAS}$	$\overline{CAS}/\overline{WE}$		WM	Color	
CBRS (Note 1,3)	0	X	0	1	-	Stop	-	X	-	-	-	-	CBR Refresh / Stop (No reset)
CBRN (Note 1)	0	X	1	1	-	X	-	X	-	-	-	-	CBR Refresh (No reset)
CBRR (Note 1)	0	X	X	0	-	X	-	X	-	-	-	-	CBR Refresh (Option reset)
MWT	1	0	0	0	X	Row	Tap	WMi	-	Yes	Load /Use	-	Masked Write Transfer (New / Old)
MSWT	1	0	0	1	X	Row	Tap	WMi	-	Yes	Load /Use	-	Masked Split Write Transfer (New / Old)
RT	1	0	1	0	X	Row	Tap	-	-	-	-	-	Read Transfer
SRT	1	0	1	1	X	Row	Tap	-	-	-	-	-	Split Read Transfer
RWM	1	1	0	0	0	Row	Col.	WMi	Data	Yes	Load /Use	-	Read Write (New / Old Mask)
BWM	1	1	0	0	1	Row	Col.	WMi	Col. Mask	Yes	Load /Use	Use	Block Write (New / Old Mask)
FWM	1	1	0	1	X	Row	X	WMi	X	Yes	Load /Use	Use	Flash Write (New / Old Mask)
RW	1	1	1	0	0	Row	Col.	X	Data	No	-	-	Read Write (No Mask)
BW	1	1	1	0	1	Row	Col.	X	Col.Mask	No	-	Use	Block Write (No Mask)
LMR (Note 2)	1	1	1	1	0	Row	X	X	WMi	-	Load	-	Load (Old) Mask Register set Cycle
LCR	1	1	1	1	1	Row	X	X	Color	-	-	Load	Load Color Register

X : Don't Care, - : Not Applicable , Tap: SAM Start(column)Address
$\overline{RAS}$ only refresh does not reset Stop or LMR functions.

Notes :

(1) CBRS, CBRN and CBRR all perform $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles. CBRR is used to reset all options and either CBRS or CBRN is used to continue to refresh the RAM without clearing any of the options.
(2) After LMR cycle, FLW, MWT, MSWT, RWM and BWM use old mask. (CBRR reset to new mask. Use CBRS or CBRN to perform $\overline{CAS}$- before-$\overline{RAS}$ refresh while using Old mask)
(3) With CBRS, all SAM operations use Stop Register.
(4) Stop defines the column on which shift out moves to the other half of the SAM.
(5) After LMR, WMi is only changed by LMR. (CBRR resets)

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on Supply Relative to Vss	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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RECOMMENDED OPERATING CONDITIONS (Voltage reference to Vss, T_A = 0 to 70 ℃)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	6.5	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

INPUT/OUTPUT CURRENT (Recommended operating conditions unless otherwise noted.)

Item	Symbol	Min	Max	Unit
Input Leakage Current (Any Input $0 \le V_{IN} \le 6.5V$, all other pins not under test=0 volts, $\overline{SE} \ge V_{CC}-0.2V$	I_{IL}	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \le V_{OUT} \le 6.5V$)	I_{OL}	-10	10	μA
Output High Voltage Level (RAM I_{OH}=-2mA, SAM I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (RAM I_{OL}=2mA, SAM I_{OL}=2mA)	V_{OL}	-	0.4	V

CAPACITANCE (T_A=25 ℃)

Item	Symbol	MIN	Max	Unit
Input Capacitance (A_0-A_8)	C_{IN1}	2	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WB}/\overline{WE}$, $\overline{DT}/\overline{OE}$, $\overline{SE}$, SC, DSF)	C_{IN2}	2	7	pF
Input/Output Capacitance (W_0/DQ_0~W_7/DQ_7)	C_{DQ}	2	7	pF
Input/Output Capacitance (SDQ_0~SDQ_7)	C_{SDQ}	2	7	pF

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter(RAM Port)	SAM Port	Symbol	KM428C258			Unit
			-6	-7	-8	
Operating Current*1 (RAS and CAS Cycling @tRC=min.)	Standby	I_{CC1}	110	100	90	mA
	Active	I_{CC1A}	155	140	125	mA
Standby Current (RAS, CAS, DT/OE, WB/WE=V_{IH},DSF=V_{IL})	Standby	I_{CC2}	10	10	10	mA
	Active	I_{CC2A}	55	50	45	mA
RAS Only Refresh Current*1 (CAS=V_{IH}, RAS Cycling @tRC=min.)	Standby	I_{CC3}	100	90	80	mA
	Active	I_{CC3A}	145	130	115	mA
Extended Fast Page Mode Current*1 (RAS=V_{IL}, CAS Cycling @tPC=min.)	Standby	I_{CC4}	80	75	70	mA
	Active	I_{CC4A}	125	115	105	mA
CAS-Before-RAS Refresh Current*1 (RAS and CAS Cycling @tRC=min.)	Standby	I_{CC5}	90	85	80	mA
	Active	I_{CC5A}	135	125	115	mA
Data Transfer Current*1 (RAS and CAS Cycling @tRC=min.)	Standby	I_{CC6}	140	125	110	mA
	Active	I_{CC6A}	185	165	145	mA
Flash Write Cycle Current*1 (RAS and CAS Cycling @tRC=min.)	Standby	I_{CC7}	90	85	80	mA
	Active	I_{CC7A}	135	125	115	mA
Block Write Cycle Current*1 (RAS and CAS Cycling @tRC=min.)	Standby	I_{CC8}	110	105	100	mA
	Active	I_{CC8A}	155	145	135	mA
Color Register Load or Read Current*1 (RAS and CAS Cycling @tRC=min.)	Standby	I_{CC9}	90	85	80	mA
	Active	I_{CC9A}	135	125	115	mA

Note *1 : Real values dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as average current.

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, V_{CC}=5.0V±10%, See notes 1,2)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	110		130		150		ns	
Read-modify-write cycle time	tRWC	155		175		200		ns	
Fast page mode cycle time	tPC	30		35		40		ns	
Fast page mode read-modify-write	tPRWC	80		85		90		ns	
Access time from RAS	tRAC		60		70		80	ns	3,5,11
Access time from CAS	tCAC		10		15		20	ns	3,5,6
Access time from column address	tAA		30		35		40	ns	3,11
Access time from CAS precharge	tCPA		35		40		45	ns	3
Write command pulse width	tWPZ	10		10		10		ns	
Write command output buffer turn-off delay	tWEZ		10		15		15	ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6 Min	-6 Max	-7 Min	-7 Max	-8 Min	-8 Max	Unit	Notes
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		3		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	15	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	10	10K	15	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	5,6
$\overline{RAS}$ to column addr. delay time	t_{RAD}	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}	10		10		10		ns	
Output hold time from $\overline{CAS}$	t_{DOH}	5		5		5		ns	
Row addr. set-up time	t_{ASR}	0		0		0		ns	
Row Addr. hold time	t_{RAH}	10		10		10		ns	
Column addr. set-up time	t_{ASC}	0		0		0		ns	
Column addr. hold time	t_{CAH}	15		15		15		ns	
Column addr. hold referenced to $\overline{RAS}$	t_{AR}	50		55		60		ns	
Column addr. to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	10		15		15		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	45		55		60		ns	
Write command pulse width	t_{WP}	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		20		ns	
Data set-up time	t_{DS}	0		0		0		ns	10
Data hold time	t_{DH}	15		15		15		ns	10
Data hold referenced to $\overline{RAS}$	t_{DHR}	50		55		60		ns	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	40		45		45		ns	8
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	85		95		105		ns	8
Column addr. to $\overline{WE}$ delay time	t_{AWD}	55		60		65		ns	8
$\overline{CAS}$ set-up time (C-B-R refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time (C-B-R refresh)	t_{CHR}	10		10		10		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	15		20		20		ns	
Access time from output enable	t_{OEA}		15		20		20	ns	
Output enable to data input delay	t_{OED}	15		15		15		ns	
Output buffer turn-off delay time from $\overline{OE}$	t_{OEZ}	0	15	0	15	0	15	ns	7
Output enable command hold time	t_{OEH}	15		15		15		ns	
Data to $\overline{CAS}$ delay	t_{DZC}	0		0		0		ns	
Data to output enable delay	t_{DZO}	0		0		0		ns	
Refresh period(512 cycle)	t_{REF}		8		8		8	ms	
$\overline{WB}$ set-up time	t_{WSR}	0		0		0		ns	
$\overline{WB}$ hold time	t_{RWH}	10		10		15		ns	
DSF hold time referenced to $\overline{RAS}$(II)	t_{FHR}	45		55		60		ns	13
DSF set-up time referenced to $\overline{RAS}$	t_{FSR}	0		0		0		ns	
DSF hold time referenced to $\overline{RAS}$(I)	t_{RFH}	10		10		15		ns	13
DSF set-up time referenced to $\overline{CAS}$	t_{FSC}	0		0		0		ns	
DSF hold time referenced to $\overline{CAS}$	t_{CFH}	10		15		15		ns	
Write per bit mask data set-up time	t_{MS}	0		0		0		ns	
Write per bit mask data hold time	t_{MH}	15		15		15		ns	
$\overline{DT}$ high set-up time	t_{THS}	0		0		0		ns	
$\overline{DT}$ high hold time	t_{THH}	10		10		15		ns	
$\overline{DT}$ low set-up time	t_{TLS}	0		0		0		ns	
$\overline{DT}$ low hold time	t_{TLH}	10		10		15		ns	
$\overline{DT}$ low hold ref. to $\overline{RAS}$(real time read transfer)	t_{RTH}	50		60		65		ns	
$\overline{DT}$ low hold ref. to $\overline{CAS}$(real time read transfer)	t_{CTH}	15		20		25		ns	
$\overline{DT}$ low hold ref. to col.addr.(real time read transfer)	t_{ATH}	20		25		35		ns	
$\overline{SE}$ setup referenced to $\overline{RAS}$	t_{ESR}	0		0		0		ns	
$\overline{SE}$ hold time referenced to $\overline{RAS}$	t_{REH}	10		10		15		ns	
$\overline{DT}$ to $\overline{RAS}$ precharge time	t_{TRP}	40		50		60		ns	
$\overline{DT}$ precharge time	t_{Tp}	20		20		20		ns	
$\overline{RAS}$ to first SC delay(read transfer)	t_{RSD}	60		70		80		ns	
$\overline{CAS}$ to first SC delay(read transfer)	t_{CSD}	25		30		35		ns	
Col.Addr.to first SC delay(read transfer)	t_{ASD}	30		35		40		ns	
Last SC to $\overline{DT}$ lead time	t_{TSL}	5		5		5		ns	
$\overline{DT}$ to first SC delay time(read transfer)	t_{TSD}	10		10		15		ns	
Last SC to $\overline{RAS}$ set-up time(serial input)	t_{SRS}	30		30		30		ns	
$\overline{RAS}$ to first SC delay time(serial input)	t_{SRD}	20		20		25		ns	
$\overline{RAS}$ to serial input delay time	t_{SDD}	30		40		50		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Serial output buffer turn-off delay from $\overline{RAS}$	t_{SDZ}	10	30	10	30	10	35	ns	
Serial input to first SC delay time	t_{SZS}	0		0		0		ns	
SC cycle time	t_{SCC}	18		22		25		ns	15
SC pulse width(SC high time)	t_{SC}	5		7		7		ns	
SC precharge(SC low time)	t_{SCP}	5		7		7		ns	
Access time from SC	t_{SCA}		15		17		20	ns	4
Serial output hold time from SC	t_{SOH}	5		5		5		ns	
Serial input set-up time	t_{SDS}	0		0		0		ns	
Serial input hold time	t_{SDH}	10		15		15		ns	
Access time from $\overline{SE}$	t_{SEA}		15		17		20	ns	4
$\overline{SE}$ pulse width	t_{SE}	20		20		25		ns	
$\overline{SE}$ precharge time	t_{SEP}	20		20		25		ns	
Serial output turn-off from $\overline{SE}$	t_{SEZ}	0	15	0	15	0	15	ns	7
Serial input to $\overline{SE}$ delay time	t_{SZE}	0		0		0		ns	
Serial write enable set-up time	t_{SWS}	0		0		0		ns	
Serial write enable hold time	t_{SWH}	10		15		15		ns	
Serial write disable set-up time	t_{SWIS}	0		0		0		ns	
Serial write disable hold time	t_{SWIH}	10		15		15		ns	
Split transfer set-up time	t_{STS}	20		25		25		ns	
Split transfer hold time	t_{STH}	20		25		25		ns	

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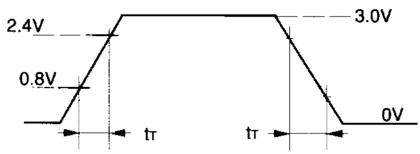
NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$, 8 SC cycles before proper device operation is achieved. ($\overline{DT}/\overline{OE}$ = High) If the internal refresh counter is used a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles are required instead of 8 $\overline{RAS}$ cycles.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max), and are assumed to be 5ns for all input signals.
   Input signal transition from 0V to 3V for AC timing.
3. RAM port outputs are measured with a load equivalent to 1 TTL load and 50pF.
   D_{OUT} comparator level:V_{OH}/V_{OL} =2.0V / 0.8V
4. SAM port outputs are measured with a load equivalent to 1 TTL load and 30pF.
   Dout comparator level: V_{OH}/V_{OL}= 2.0/0.8V.
5. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. The t_{RCD}(max) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
6. Assumes that $t_{RCD} \geq t_{RCD}$(max).
7. The parameters, t_{OFF}(max), t_{OEZ}(max), and t_{SDZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to V_{OH} or V_{OL}.
8. The t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are nonrestrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the CAS leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insured that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. After power-up, initial status of chip is described below

PIN or REGISTER	STATUS
Color Register	Don't Care
Write Mask Register	Don't Care
Tap Pointer	Invalid
Stop Register	Default Case
Wi/DQi	Hi-Z
SAM Port	Input Mode
SDQi	Hi-Z

13. (I) DSF hold time at the falling edge of $\overline{RAS}$
    (II) DSF hold time at the falling edge of $\overline{CAS}$
14. Recommended operating input condition :



Input pulse levels are from 0.0V to 3.0Volts.
All timing measurements are referenced from V_{IL} (max) and V_{IH} (min) with transition time = 3.0ns

15. Assume t_T = 3.0ns

DEVICE OPERATION

The KM428C258 contains 2,097,152 memory locations. Eighteen address bits are required to address a particular 18 bit word in the memory array. Since the KM428C258 has only 9 address input pins, time multiplexed addressing is used to input 9 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe($\overline{RAS}$), the column address strobe($\overline{CAS}$)and the valid row and column address inputs.

Operation of the KM428C258 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 9 address input pins are changed from a row address to a column address and are strobed in by $\overline{CAS}$. This is the beginning of any KM428C258 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time(t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS} (min) and t_{CAS} (min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM428C256 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirement, loss of data integrity can occur.

RAM Read

A RAM read cycle is achieved by maintaining $\overline{WB}/\overline{WE}$ high during a $\overline{RAS}$ / $\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition.

If $\overline{CAS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD} (max) then the access time to valid data is specified by t_{RAC} (min). However, if $\overline{CAS}$ goes low after t_{RCD} (max) or the column address becomes valid after t_{RAD} (max), access time is specified by t_{CAC} or t_{AA}.

The KM428C258 has common data I/O pins. The $\overline{DT}/\overline{OE}$ has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, $\overline{DT}/\overline{OE}$ must be low for the period of time defined by t_{OEA}.

Extended Data Out

In the conventional RAM Read cycle, DOUT buffer is designed to make turn-off by the rising edge of $\overline{CAS}$ even though $\overline{OE}$ is to be low. But the KM428C258 can be improved the cycle time of fast page mode(t_{PC})than existed using new scheme do no do no disable by the rising edge of $\overline{CAS}$. This is called "Extended Data Output(or Hyper Page) mode", which makes valid. Data during $\overline{CAS}$ high period. This mode can be performed in any RAM Fast page cycle and the case of disabling. DOUT is achieved respectively during write mode, $\overline{DT}/\overline{OE}$ = high period, and also often t_{off} time determined by activating firstly one of two edge. In have, if write mode is available, data buffer was designed to turn-off before enabling by $\overline{CAS}$ when read cycle is performed again. What the output buffer is disabling during $\overline{DT}/\overline{OE}$ = high is to use bank selection in the frame buffer memory using common I/O line.

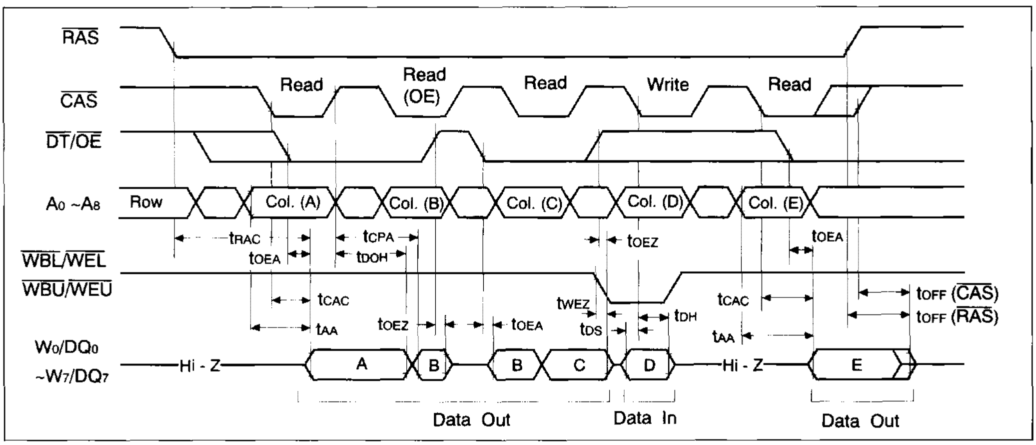


Figure 1. Fast Page Mode (Extended Data Output) Example

DEVICE OPERATION (Continued)

Nibble Write Operation

The KM28C258 is possible asynchronous operation with lower nibble(0~3)and upper nibble(4~7), which has write control pin with $\overline{WBL}/\overline{WEL}$ and $\overline{WBU}/\overline{WEU}$. This is called 'Nibble Write Operation' function, which is possible operation in cycle as RAM write, Block Write, Load mask register, and Load Color register.

New Mask Write Per Bit

The New Mask Write cycle is achieved by maintaining $\overline{CAS}$ high and $\overline{WBX}/\overline{WEX}$ and DSF low at the falling edge of RAS. The mask data on the W_0/DQ_0~W_7/DQ_7 pins are latched into the write mask register at the falling edge of $\overline{RAS}$. When the mask data a low, writing is inhibited into the RAM and the data bit remains unchanged. When the mask data is high, data is written into the RAM. The mask data is valid for only one cycle, defined by an active $\overline{RAS}$ period. Mask data must be provided in every write cycle that a masking operation is desired.

The Early Write cycle is achieved by $\overline{WBX}/\overline{WEX}$ low before $\overline{CAS}$ falling and Late Write cycle is achieved by $\overline{WBX}/\overline{WEX}$ high at the falling edge of $\overline{CAS}$. During the Early or Late Write cycle, input data through W_0/DQ_0~W_7/DQ_7 must meet the set-up and hold time at the falling edge of $\overline{CAS}$ or $\overline{WBX}/\overline{WEX}$. When $\overline{WBX}/\overline{WEX}$ is high at the falling edge of RAS no masking operation is performed.

Table 1. Truth table for write-per-bit function

$\overline{RAS}$	$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	Wi/DQi	FUNCTION
↘ (falling)	H	H	H	*	WRITE ENABLE
	H	H	L	1	WRITE ENABLE
				0	WRITE MASK

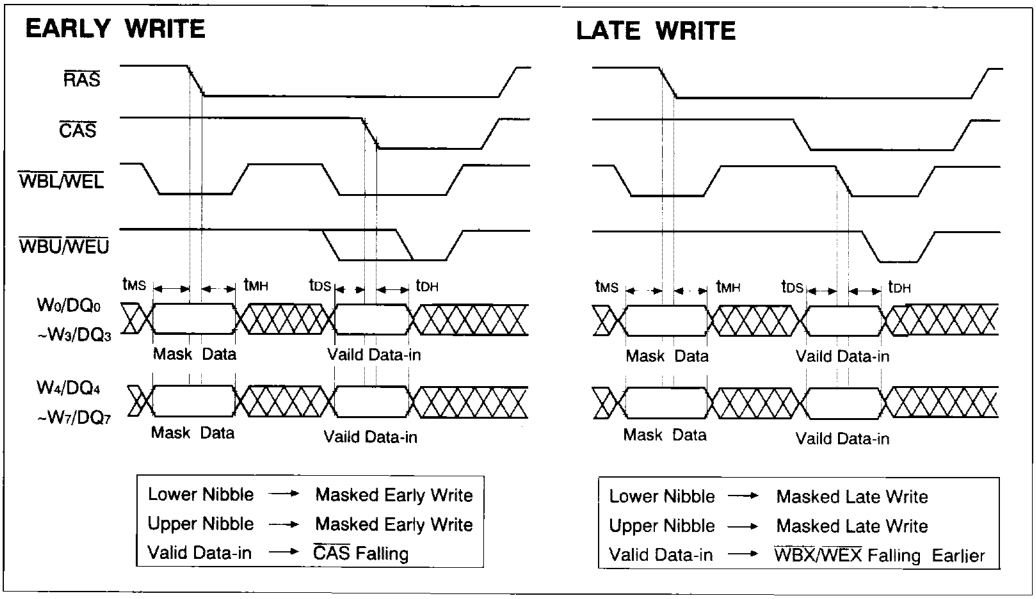


Figure 2. Nibble Write and New Masked Write Cycle Example 1 (Early Write & Late Write)

DEVICE OPERATION (Continued)

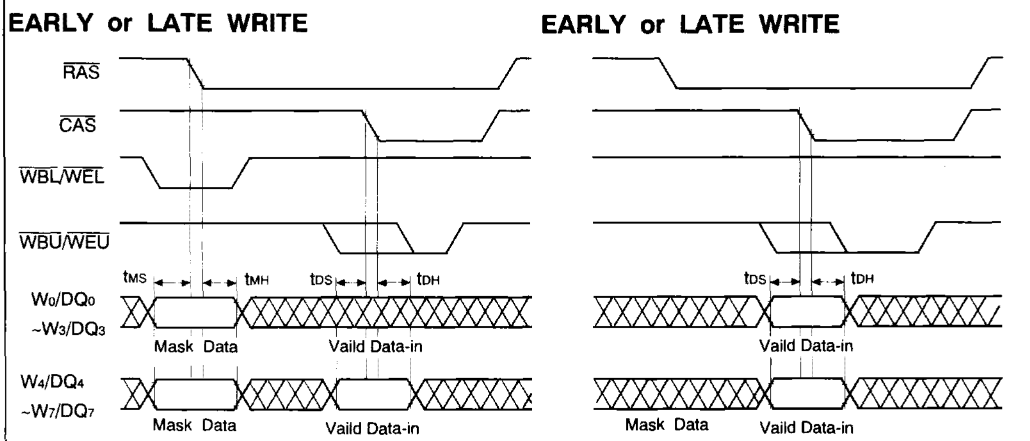
Old Mask Write Per Bit

This mode is enabled through the load mask register(LMR) cycle. The I/O mask data during old masked WPB cycle, remains unless I/O mask data is changed by the another LMR cycle. The condition of LMR cycle is DSF high at the falling edge of RAS and DSF low at the falling edge of CAS during normal write cycle. Mask data is synchronized by falling of WBL/WEL and WBU/WEU and CAS edges and this data is latched through W_0/DQ_0~W_7/DQ_7.

The difference between old masked write cycle and new masked write cycle is ignoring input data all the RAS falling edge during old masked write.

Old masked write mode is converted to new masked write mode by the CBR refresh with optional reset cycle (CBRR).

CBRR cycle can be achieved by lowering DSF at the RAS falling edge of CBR cycle. Masking mode after power up is initialized to new masked write mode.



If Early Write	
Lower Nibble →	No Write
Upper Nibble →	Masked Early Write
Valid Data-in →	CAS Falling

If Late Write	
Lower Nibble →	No Write
Upper Nibble →	Masked Late Write
Valid Data-in →	WBX/WEX Falling

If Early Write	
Lower Nibble →	No Data Load
Upper Nibble →	Non Masked Late Write
Valid Data-in →	CAS Falling

If Late Write	
Lower Nibble →	No Data Load
Upper Nibble →	Non Masked Late Write
Valid Data-in →	WBX/WEX Falling

Figure 3. Nibble Write and New Mask Write Cycle Example 2

DEVICE OPERATION (Continued)

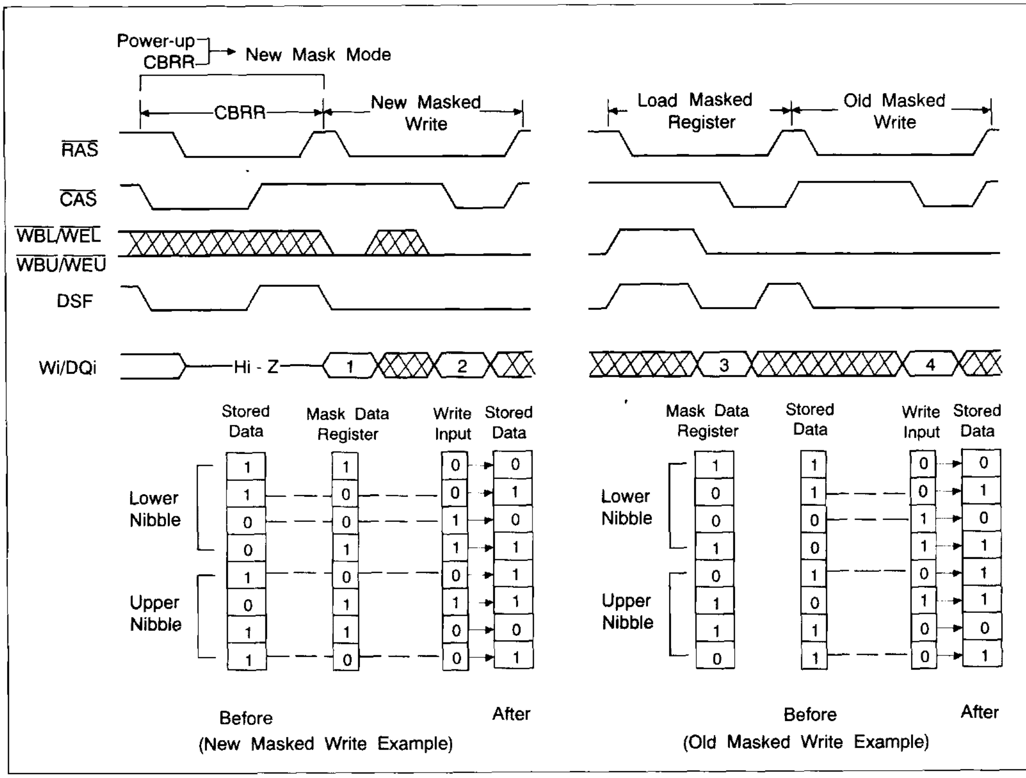


Figure 4. New Mask Write Cycle and Old Mask Write Cycle Example

Fast Page Mode

Fast page mode cycle reads/writes the data of the same row address at high speed by toggling $\overline{CAS}$ while $\overline{RAS}$ is low. It's cycle time is less then one third of the random read/write cycle(t_{RC}). In this cycle, read, write, read-modify write, and block write cycles can be mixed. In one $\overline{RAS}$ cycle, 512 word memory cells of the same row address can be accessed. Masking data stored by $\overline{RAS}$ falling of fast page or load mask register cycle is subsequently valid during the persistent fast page write cycles.

Load Color Register(LCR)

A Load Color Register cycle is performed by keeping DSF high on the both the falling edges of $\overline{RAS}$ and $\overline{CAS}$. Color data is loaded on the falling edge of CAS(early write) or $\overline{WE}$(delayed write) via the W_0/DQ_0~W_7/DQ_7 pins. This data is used in Block Write and Flash Write cycles and remains unchanged until the next Load Color Register cycle.

Block Write

In a Block Write cycle four adjacent column locations can be written simultaneously with the same data, resulting in fast screen fills of the same color.

First, the internal 8-bit Color Register must be loaded with the data to be written by performing a Load Color Register(LCR) cycle. When a Block Write cycle is performed, each bit of the Color Register is written into four adjacent locations of the same row of each corresponding bit plane(8). This results in a total of 32-bits being written in a single Block Write cycle compared to 8-bits in a normal Write cycle.
The Block Write cycle is performed if DSF is low on the falling edge of $\overline{RAS}$ and high on the falling edge of $\overline{CAS}$.
Address Lines: The row address is latched on the falling edge of RAS.

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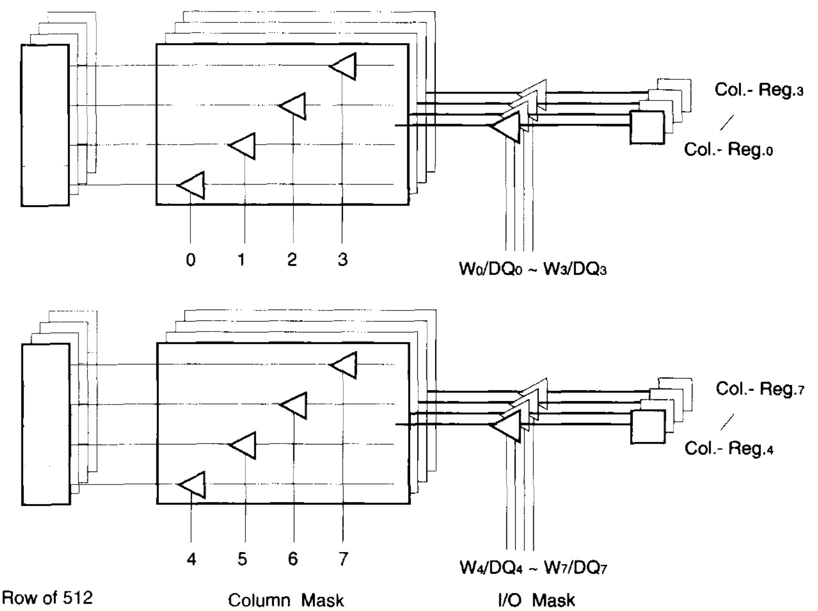
DEVICE OPERATION (Continued)



	$\overline{RAS}$ ↓
$W_0/DQ_{0\sim3}$	Lower Block I/O Mask
$W_4/DQ_{4\sim7}$	Upper Block I/O Mask

	$\overline{CAS}$ ↓
$A_0 \sim A_2$	Don't Care
$W_0/DQ_{0\sim7}$	Use to Column Select

A_0	A_1	Lower	Upper	Column Mask	
0	0	W_0/DQ_0	W_4/DQ_4	DQi = 1	Column Enable
0	1	W_1/DQ_1	W_5/DQ_5		
1	0	W_2/DQ_2	W_6/DQ_6	DQi = 0	Column Disable
1	1	W_3/DQ_3	W_7/DQ_7		

Figure 5. Block Write Scheme

Since four bits are being written at a time, when the minimum increment required for the column address is four. Therefore, when the column address is latched on the falling edge of $\overline{CAS}$, the 2LSBs, A_0 and A_1 are ignored and only bits(A_2~A_8) are used to define the location of the first bit out of the four to be written.

Data Lines: On the falling edge of $\overline{CAS}$, the data on the W_0/DQ_0~W_3/DQ_3 pins provideds column mask data. That is, for each of the four bits in all 8-bits-planes, writing of Color Register contents can be inhibited. For example, if W_0/DQ_0=1 and W_0/DQ_1=0, then the Color Register contents will be written into the first bit out of the four, but the second remains unchanged. Fig 5 shows the correspondence of each data line to the column mask bits.

Masked Block Write(BWNM)

A Masked Block Write cycle is identical to a New Mask Write-per-bit cycle except that each of the 8-bit planes being masked is operating on 4 column locations instead of one.

To perform a Masked Block Write cycle, both DSF and $\overline{WB}/\overline{WE}$ must be low at the falling edge of $\overline{RAS}$. DSF must be high on the falling edge of $\overline{CAS}$. Mask data is latched into the device via the W_0/DQ_0~W_7/DQ_7 pins on the falling edge of $\overline{RAS}$ and needs to be re-entered for every new $\overline{RAS}$ cycle.

DEVICE OPERATION (Continued)

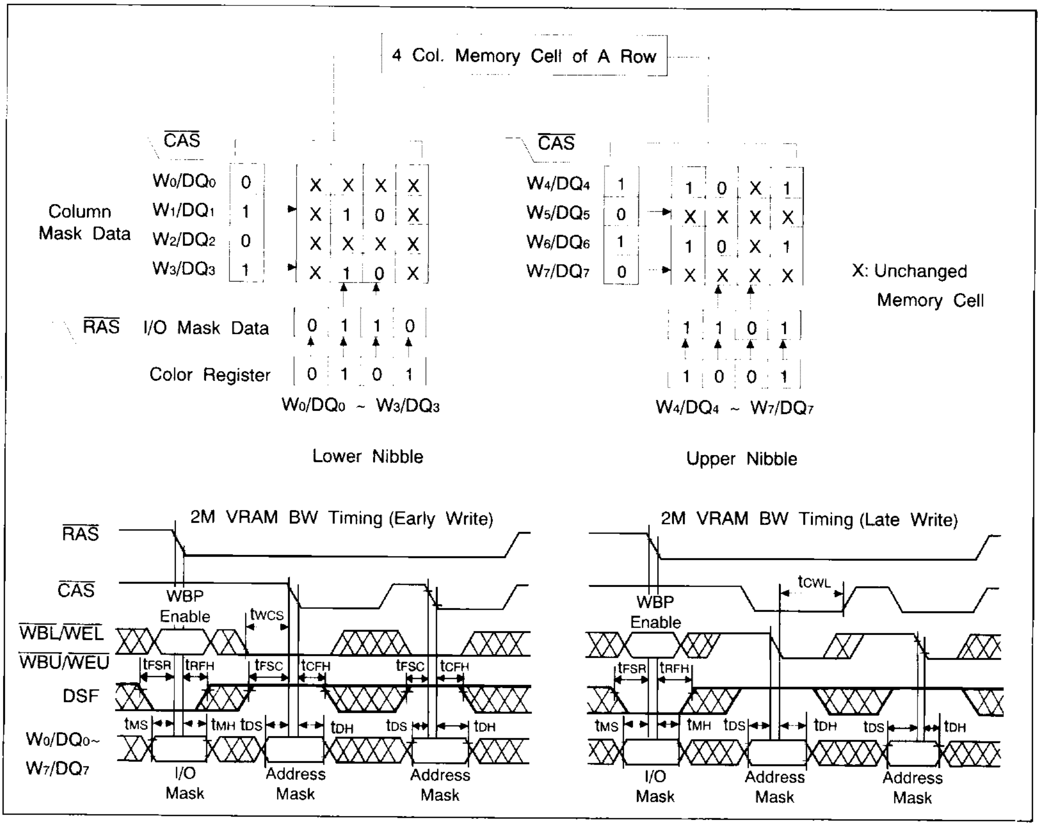


Figure 6. Block Write Example and Timing

Flash Write

The Flash Write cycle is a way of writing each bit of the Color Register into the whole row(512 columns) simultaneously. This function is used for fast screen clear or background color change. 512 columns in each bit plane are written, for a total of 4096 bits(512 × 8 bit planes) in one cycle. While this cycle writes significantly more data than the Block Write cycle, it is also less selective.

If WBX/WEX is low and DSF is high on the falling edge of RAS, a Flash Write cycle is performed. Also on this edge, the data present on the Wi/DQi pins is used as mask data and needs to be provided for every Flash Write cycle. A Load Color Register cycle must have been performed before initiating a Flash Write cycle.

Data Output

The KM428C258 has three state output buffers controlled by DT/OE, CAS and RAS, WBX/WEX. If DT/OE is high when CAS and RAS are high, the output state is in high impedance(High-z). In any cycle, the output goes low impedance state from the first CAS falling edge.
Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC}, and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until CAS returns high. This is true even if a new RAS cycle occurs(as in hidden refresh).
Each of the KM428C258 operating cycles is listed below after the corresponding output state produced by the cycle.

DEVICE OPERATION (Continued)

Refresh

The data in the KM428C258 is stored as a charge on a tiny capacitor within each memory cell. Due to leakage the data may be lost over a period of time. To maintain data integrity it is necessary to refresh each of the 512 rows every 8 ms. Any operation cycle performed in the RAM port refreshes the 4096 bits selected by the row addresses or an on-chip refresh address counter. Either a burst refresh or distributed refresh may be used. There are several ways to accomplish this.

RAS-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with RAS while CAS remains high. This cycle must be repeated for each of the 512 row addresses. (A_0~A_8).

CAS-Before-RAS Refresh: The KM428C258 has CAS-before-RAS on-chip refresh capability that eliminates the need for external refresh addresses. If CAS is held low for the specified set up time(t_{CSR}) before RAS goes low the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next CAS-before-RAS refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the CAS active time and cycling RAS. The KM428C258 hidden refresh cycle is actually a CAS before-RAS refresh cycle within an extended read cycle. The refresh row address is the provided by the on-chip refresh address counter.

Self Refresh(Only KM428C258): The Self Refresh is used for maintaining data is stand-by state of device as battery back-up function. The initialization cycle of Self Refresh can be used by cycle named CBRN, CBRR, CBRS, If RAS is row more than 100μs at the condition of CBR, Self Refresh address do not need to supply additionally on chip because the refresh counter on chip gives note that addresses needed to refresh. Please note that the ending point of Self Refresh is when RAS and CAS is high and t_{RPS} of Self Refresh is the time requesting to complete the last refresh of Self Refresh.

Other Refresh Methods: It is also possible to refresh the KM428C258 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general RAS-only or CAS-before-RAS refresh is the preferred method.

Transfer Operation

Transfer operation is initiated when DT/OE is low at the falling edge of RAS. The state of WB/WE when RAS goes low indicates the direction of transfer (to or from DRAM) and DSF pin is used to designate the proper transfer mode like normal and Split Transfer. Each of the transfer cycle is described in the truth table of transfer operation.(Table2.)

Read Transfer(RT)

The Read Transfer operation is set if DT/OE is low, WB/WE is high, and DSF is low when RAS goes low. The row address bits in the read transfer cycle indicate which eight 512bit DRAM Row portions are transferred to the eight SAM data registers. The column address bits indicate the start address of the SAM registers when SAM data read operation is performed. If MSB bit of column address is low during Read transfer operation, the start address of the SAM register is present at the lower half of the SAM port.(If A_8 high, the start address is in the upper half). Read Transfer may be achieved in two ways. If the transfer is to be synchronized with the SC, both SAM Read and Read transfer operation is possible simultaneously. The completion of transfer operation is determined by the timing relationship of first SC rising, RAS/CAS falling edge and DT/OE rising edge of transfer cycle. This is usually called "Read time Read Transfer". The completion of Real time Read transfer is accomplished at the rising edge of DT/OE. Note that the rising edge of DT/OE. Note that the rising edge of DT/OE must be synchronized with the rising edge of SC to retain the continuity of serial read data output.

Table.2 Truth Table for Transfer Operation

* : Don't care

RAS Falling Edge					Function	Transfer Direction	Transfer Data Bit	SAM Port Mode
CAS	DT/OE	WB/WE	DSF	SE				
H	L	H	L	*	Read Transfer	RAM ▸ SAM	512 x 8	Input ▸ Output
H	L	L	L	*	Masked Write Transfer	SAM ▸ RAM	512 x 8	Output ▸ Input
H	L	H	H	*	Split Read Transfer	RAM ▸ SAM	256 x 8	Not Changed
H	L	L	H	*	Masked Split Write Transfer	SAM ▸ RAM	256 x 8	Not Changed

DEVICE OPERATION (Continued)

Masked Write Transfer(MWT)

Masked write transfer is initiated if $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$ and DSF are low when $\overline{RAS}$ goes low. This enables data of SAM register(512bit) to be transferred to the selected ROW in the DRAM array. Masking is selected by latching Wi/DQi(i=0~7)inputs when $\overline{RAS}$ goes low.
The column address defines the start address of serial input.
If A_8 is low, the start address is positioned in the lower half of SAM.(For A_8=high, the start address will be positioned in the upper half of SAM) After write transfer cycle is completed, SAM port is set to input mode.

Split Read Transfer(SRT)

In a graphic system, if data has to be transferred from DRAM to SAM while in the middle of a display line, the only way to do this seamlessly is by performing a Real Time Read Transfer cycle. However, this cycle has many critical timing restrictions(between SC, $\overline{DT}/\overline{OE}$, $\overline{RAS}$ and $\overline{CAS}$) because the transfer has to occur at the first clock of the new data.

The Split Read Transfer cycle eliminates the need for this critical transfer timing, there by simplifying system design. This is accomplished by dividing the SAM port into 2 halves of 256 bits each. A Split Read Transfer loads only the lower op upper half. While data is being serially read from one half of the SAM register, new RAM data can be transferred to the other half. The transfer is not synchronized with a 1μ s period while the other half is accessing data. Since transfer timing is controlled internally, there is no timing restriction between $\overline{DT}/\overline{OE}$ and $\overline{RAS}$, $\overline{CAS}$, SC.

A normal Read Transfer cycle must be executed before performing a Split Read Transfer. A Split Read Transfer cycle is begun by keeping DSF and $\overline{WB}/\overline{WE}$ high and $\overline{DT}/\overline{OE}$ low at the falling edge of $\overline{RAS}$.

Address: The row address is latched on the falling edge of $\overline{RAS}$. The column address defined by(A_0~A_7)defines the starting address of the SAM port from which data will begin shifting out. Address pin A_8 is a "Don't care".

A Split Read Transfer will load data into the other half.
Example of SRT applications are shown in Fig. 7 through Fig 11.
The normal usage of Split Read Transfer cycle is described in Fig. 7. When Read Transfer is executed, data from X1 row address is fully transferred to the SAM port and Serial Read is started from 0(Tap address). If SRT is performed while data is being serially read from lower half SAM, data from X2 row address is transferred to upper half SAM. The Tap address of SRT is loaded after the boundary location of lower half SAM(255th SC) is accessed and the DSF state is changed into high level at the rising edge of 255 SC. Note that in this case "0+256" Tap address instead of "0" is loaded.
The another example of SRT cycle is described in Fig. 8. When Serial Read is performed after executing RT and SRT in succession the data accessed by first SC is the data of RT Tap address. Serial data access from the starting address given by SRT cycle is performed after the data of RT to lower boundary (255th SC) is completed. Fig. 9 and 10 are the example of abnormal SRT cycle. If SRT1 and SRT2 are performed in succession before accessing the boundary like Fig. 9, the data transferred by SRT2 overwrite the data transferred by SRT1, so that data followed by SRT2 will be remain in the upper half SAM. The Serial Read after lower boundary 255th SC is started from the starting address given by SRT2 cycle. The Fig.10, indicates that SRT cycle is not performed until Serial Read is completed to the boundary location 511. In this case, the internal serial counter is designed to designate "0" address after boundary 511, therefore accessed data from 0 address corresponds to the old data transferred by RT. Note that there is not allowed period of SRT cycle as shown in Fig. 11 due to uncertaining of which half SAM the data is transferred. This is also true in Masked Split Write Transfer..
A Split Read Transfer does not change the direction of the SAM I/O port.

Masked Split Write Transfer(MSWT)

This transfer function is very similiar to the SRT except the data transfer direction is from SAM to RAM. MSWT is enabled if $\overline{DT}/\overline{OE}$ low, $\overline{WB}/\overline{WE}$ low, and DSF high when $\overline{RAS}$ goes low. The bit masking of this cycle is the same as that of MWT(Masked Write Transfer)and the SAM port direction is not changed by performing MSWT. And the column address is latched in as the start address of SAM port and the MSB(A_8)is a "don't care". The example of MSWT is described in fig.10. The opening cycle of either MWT or PWT is needed before MSWT can be performed.

DEVICE OPERATION (Continued)

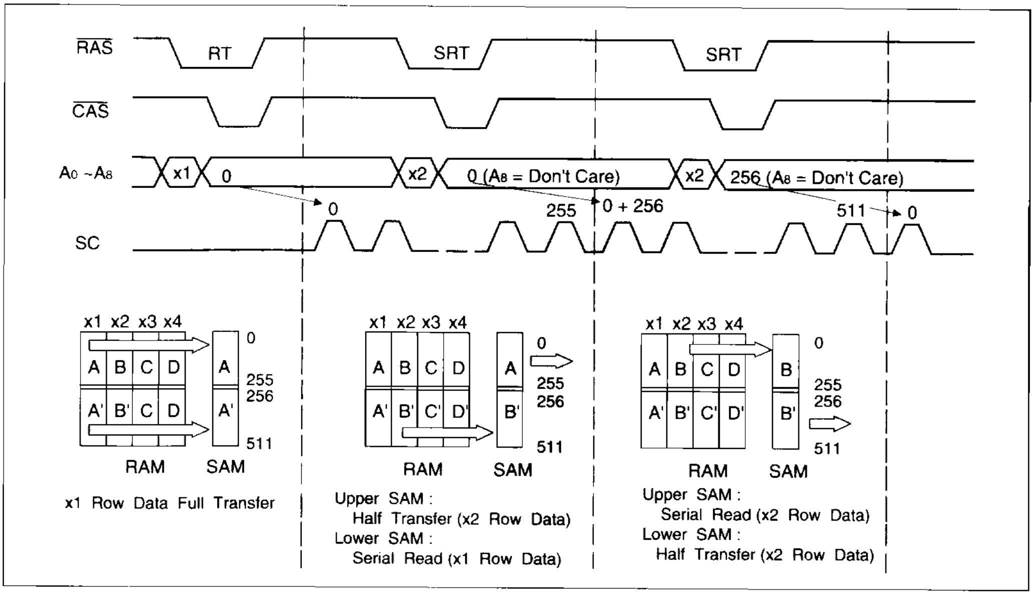


Figure 7. Split Read Transfer Normal Usage

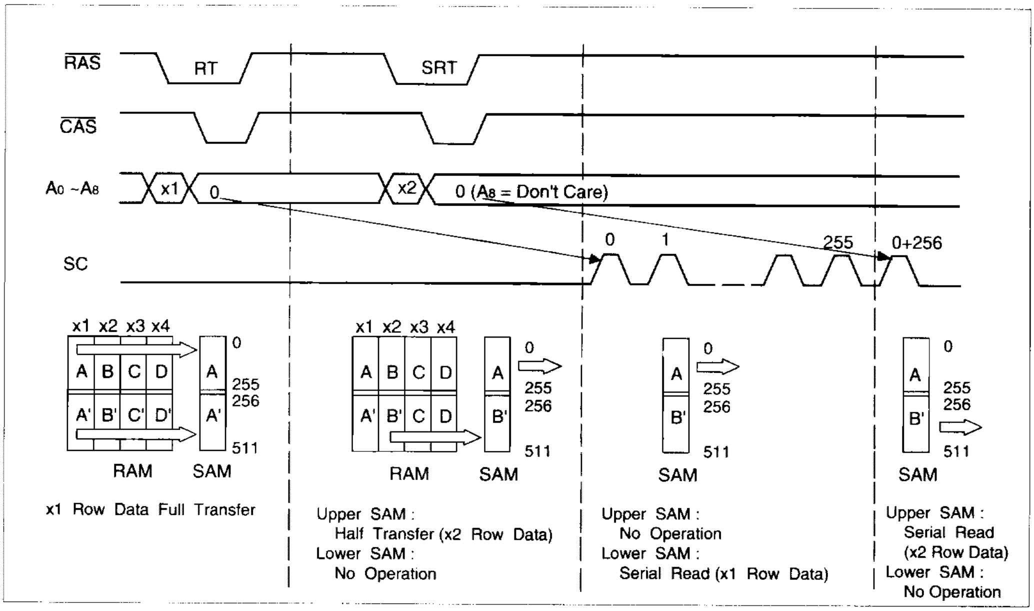


Figure 8. Split Read Transfer Normal Usage

DEVICE OPERATION (Continued)

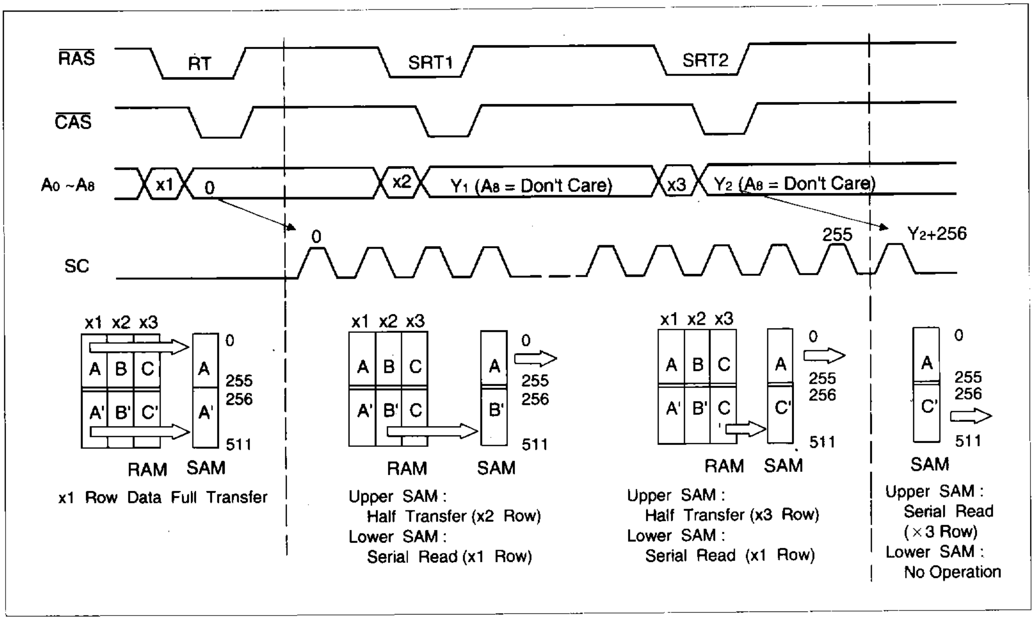


Figure 9. Split Read Transfer Abnormal Usage (Case 1)

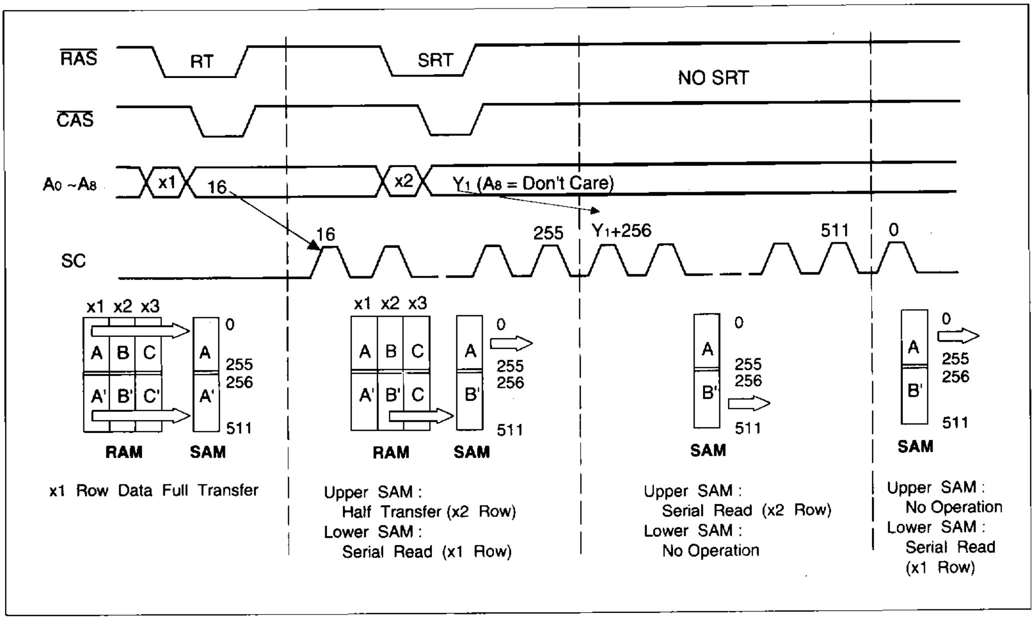


Figure 10. Split Read Transfer Abnormal Usage (Case 2)

DEVICE OPERATION (Continued)

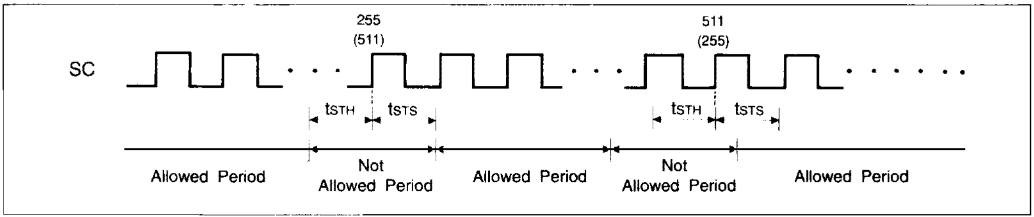


Figure 11. Split Transfer Cycle Limitation Period

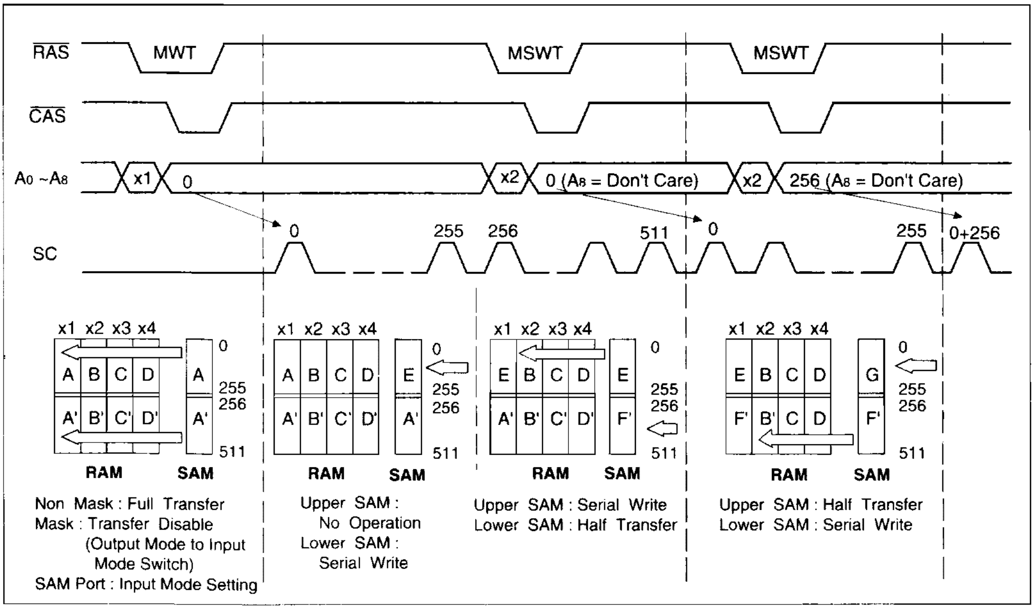


Figure 12. Masked Split Write Transfer Normal Usage

DEVICE OPERATION (Continued)

Programmable Split SAM

As the split SAM mode is divided into the lower half SAM and the upper half SAM, the Tap has jumped to the another half SAM after accessing the last address of each half SAM. Usually this last addresses is called "Stop address". Programmable Split SAM helps user to reconfigure the stop address from two(255, 511)to a maximum of 32 stop address. In fig.13 shows the condition of stop point setting address. The KM428C258 has basically two stop address(255, 511) and provides the maximum 32 stop address. These stop addresses are set into the stop register by CBRS cycle. The CBRS cycle's conditions is $\overline{WBL}/\overline{WEL}$ or $\overline{WBL}/\overline{WEL}$ low, DSF high when $\overline{RAS}$ goes low in normal CBR cycle and the stop address is determined by row address entering at this time. The stop address is valid only after split transfer is completed. In the serial read/write is operating after RT, MWT ending, the stop address do not effect to operate SAM port and when the Tap of SAM port reaches the stop address after achieving split transfer, the Tap of SAM port will be jumped to the start address of another If the split transfer is not executed before accessing the stop address, the operation of half SAM being accessed will be continued. The operation of SRT using stop address is described in the table of fig. 13.
When the stop address is set into the 4 section, splited 127, 225, 383, 511 by CBRS cycle, the serial read is starts from 351 address and jump to 70, indicating the start address of SRT1 after ending access of 383 address. Because the SRT is not performed from 70 to 127 address, the next address of SAM will be assigned to 71 address.
Note that the stop address set by CBRS can be changed to the another address by other CBRS, this new address changed will be not adapted until the next split transfer is completed. Finally, the stop address for reset is initiated by CBRR cycle, the default address of reset will be 255, 511.

Table 3. Stop Point Setting Address

Stop Register = Store the Address of Serial Access
Use on the Split Transfer Cycle
Stop Pointer Set ▸ CBRS Cycle

Number of Stop Points / Half	Partition	Stop Point Setting Address					
		A_8	A_7	A_6	A_5	A_4	$A_3 \sim A_0$
1	(1x256)x2	X	1	1	1	1	X
2	(2x128)x2	X	0	1	1	1	X
4	(4x64)x2	X	0	0	1	1	X
8	(8x32)x2	X	0	0	0	1	X
16	(16x16)x2	X	0	0	0	0	X
T	(TxWidth)x2	Other Case = Inhibit					

Stop Address = (i + Width) - 1 (i = 0 ----- T + 1)

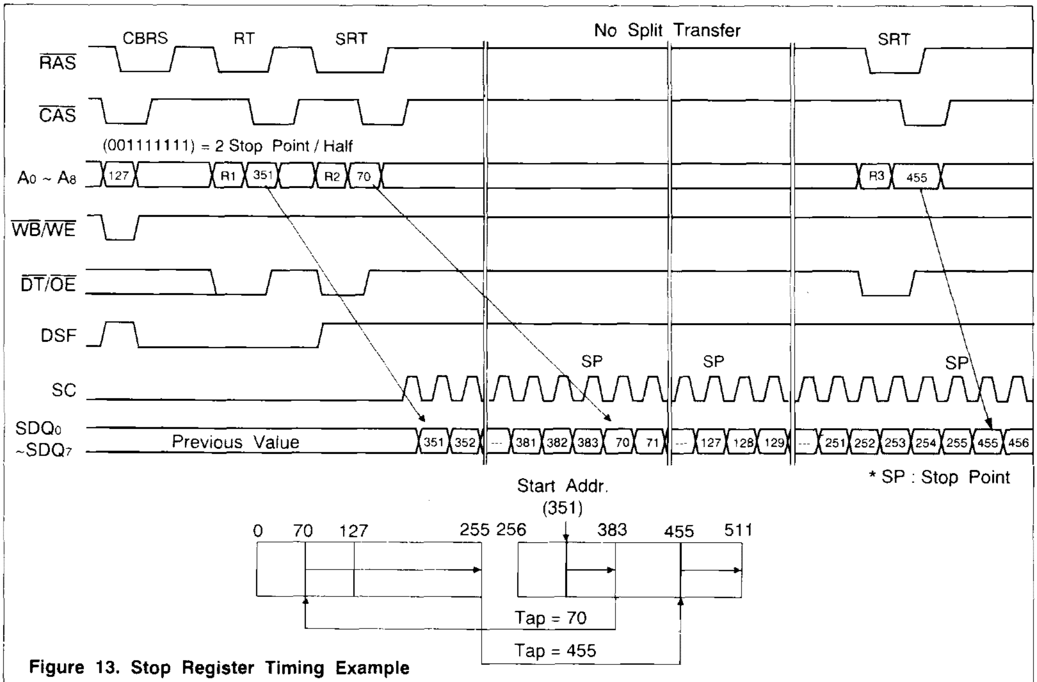
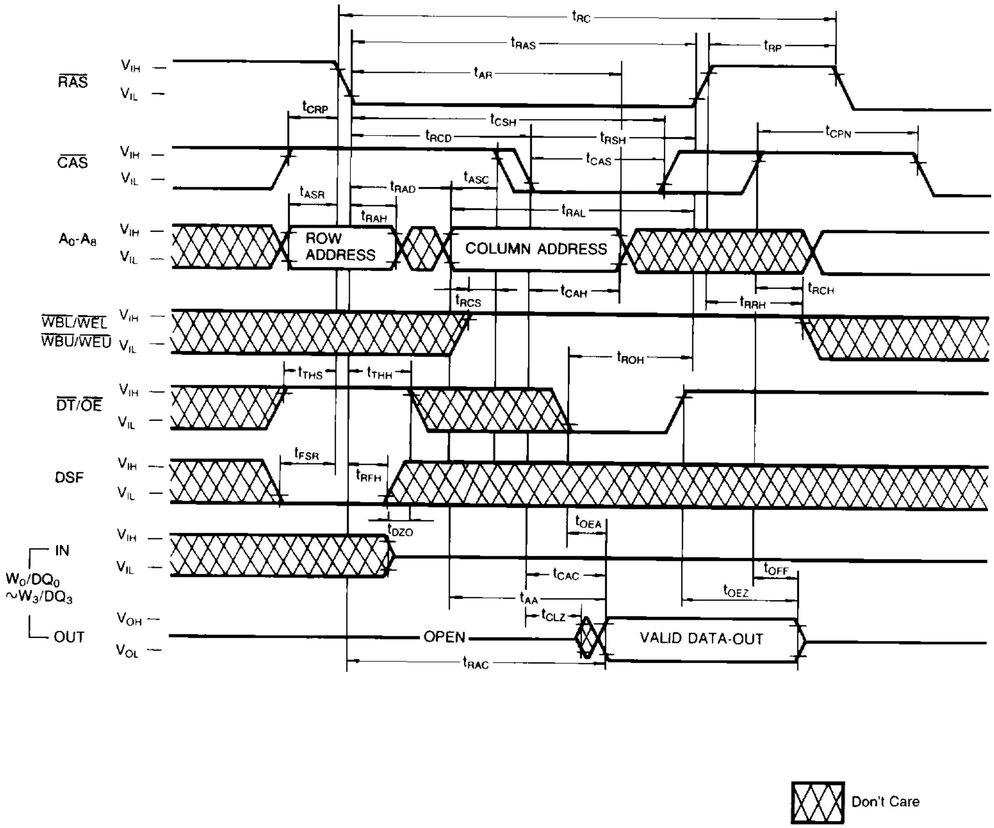


Figure 13. Stop Register Timing Example

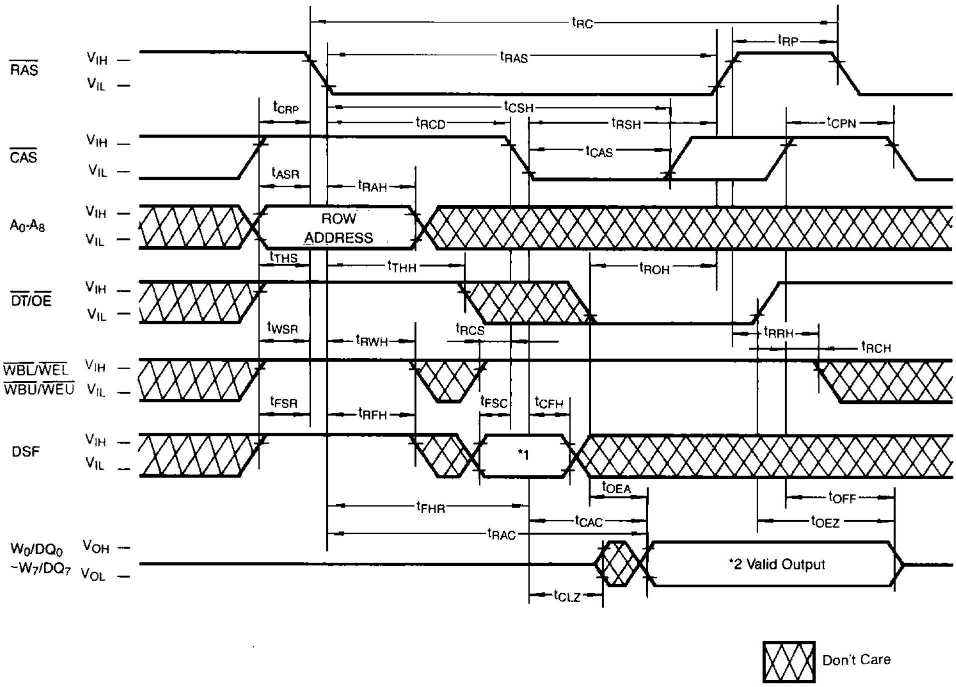
TIMING DIAGRAMS (Continued)

READ CYCLE



TIMING DIAGRAMS (Continued)

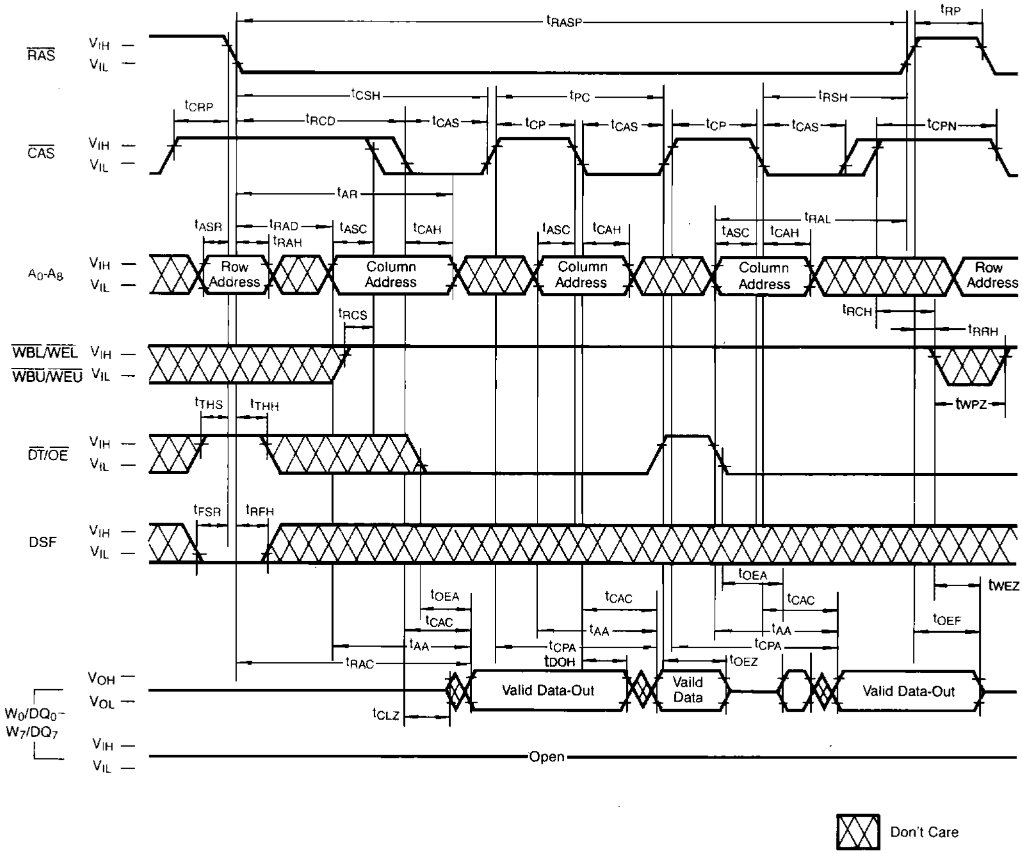
READ MASK/COLOR REGISTER CYCLE



*1	*2	Fuction
0	Mask data	Read Mask Register Cycle
1	Color data	Read Color Register Cycle

TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ CYCLE (Extended Data Out)



TRUTH TABLE FOR WRITE CYCLE(1)

FUNCTION	$\overline{RAS}$ ↘			$\overline{CAS}$ (3) ↘	
	*1 $\overline{WBL}$/WBL (WBU/WEU)	*2 DSF	*3 Wi/DQi (4) (New Mask)	*4 DSF	*5 Wi/DQi
Normal Write	1	0	X	0	Write Data
Masked Write	0	0	Write Mask	0	Masked Write Data
Block Write (No I/O Mask)(5)	1	0	X	1	Column Mask
Masked Block Write(5)	0	0	Write Mask	1	Column Mask
Masked Flash Write	0	1	Write Mask	X	X
Load Mask Data Register(2)	1	1	X	0	Write Mask Data
Load Color Register	1	1	X	1	Color Data

Note : (1) Reference truth table to determine the input signal states of *1, *2, *3, *4, and *5 for the write cycle timing diagram
(2) Old Mask data load
(3) On the Masked Flash Write cycle, all the signal inputs are don't care condition except $\overline{RAS}$ at the falling edge of $\overline{CAS}$.
(4) Function table for Old Mask and New Mask

IF		*1		*3	Note
		$\overline{WBL}$/WBL	$\overline{WBU}$/WEU	Wi/DQi	
LMR Cycle Executed	Yes	X	X	X	Write using mask register data (Old Mask Data)
	No	0	0	Write Mask	Write using New Mask Data
		0	1		Wi/DQi = 0 → Write Disable
		1	0		Wi/DQi = 1 → Write Enable
		1	1	X	Non Masked Write

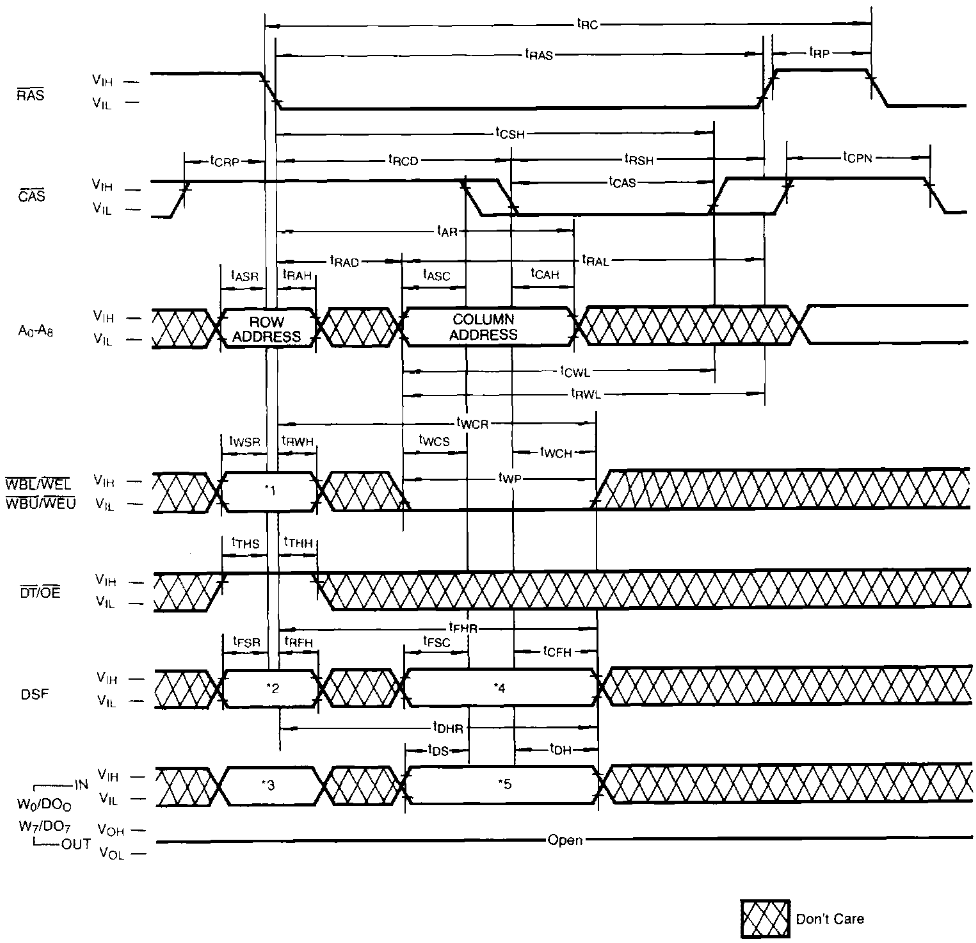
X : Don't Care

(5) Function Table for Block Write Column Mask

Column Address			*5		IF	
A_1	A_0		Lower Nibble	Upper Nibble	Wi/DQi=0	Wi/DQi=1
0	0	→	W_0/DQ_0	W_4/DQ_4	No Change the Internal Data	Color Register Data are Write to the Corresponding Column Address Location
0	1	→	W_1/DQ_1	W_5/DQ_5		
1	0	→	W_2/DQ_2	W_6/DQ_6		
1	1	→	W_3/DQ_3	W_7/DQ_7		

TIMING DIAGRAMS (Continued)

EARLY WRITE CYCLE



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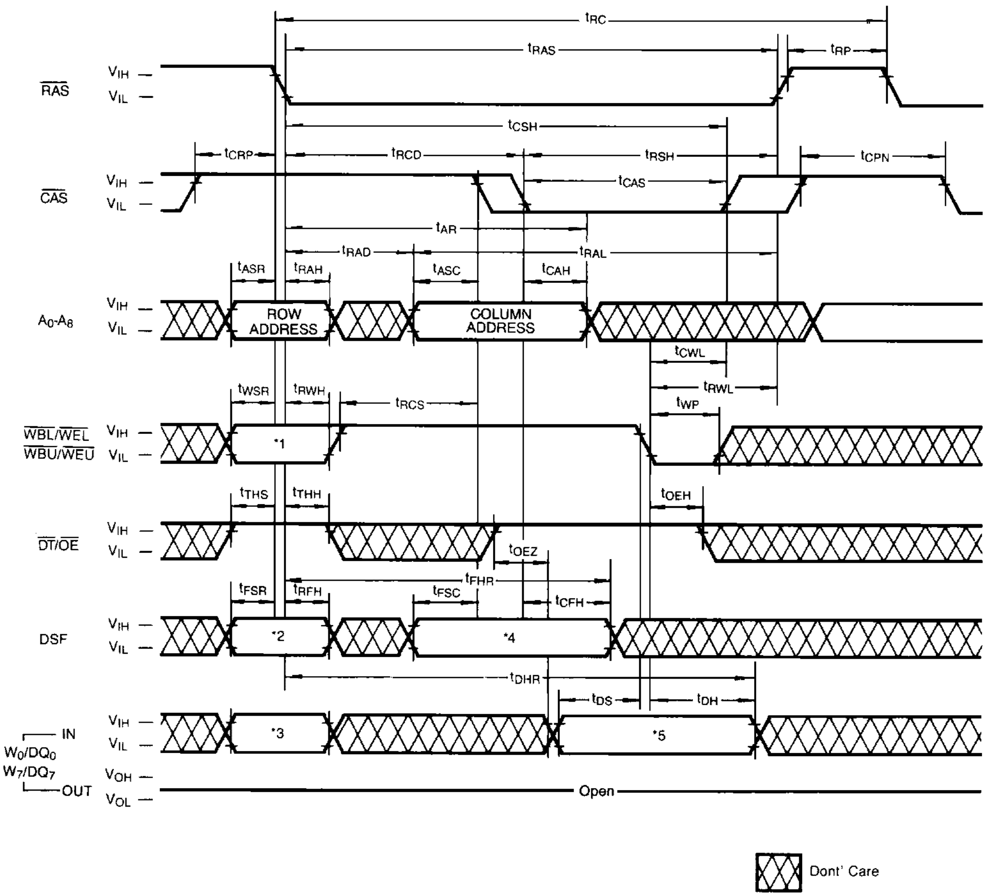
SAMSUNG ELECTRONICS

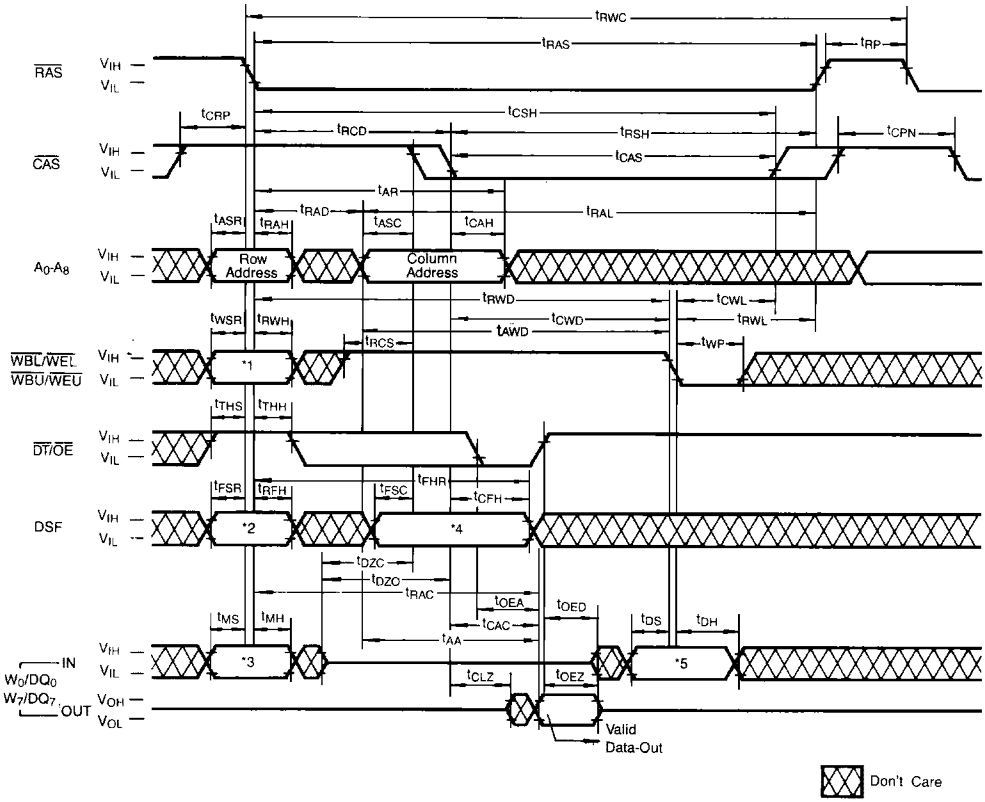
TIMING DIAGRAMS (Continued)

LATE WRITE CYCLE



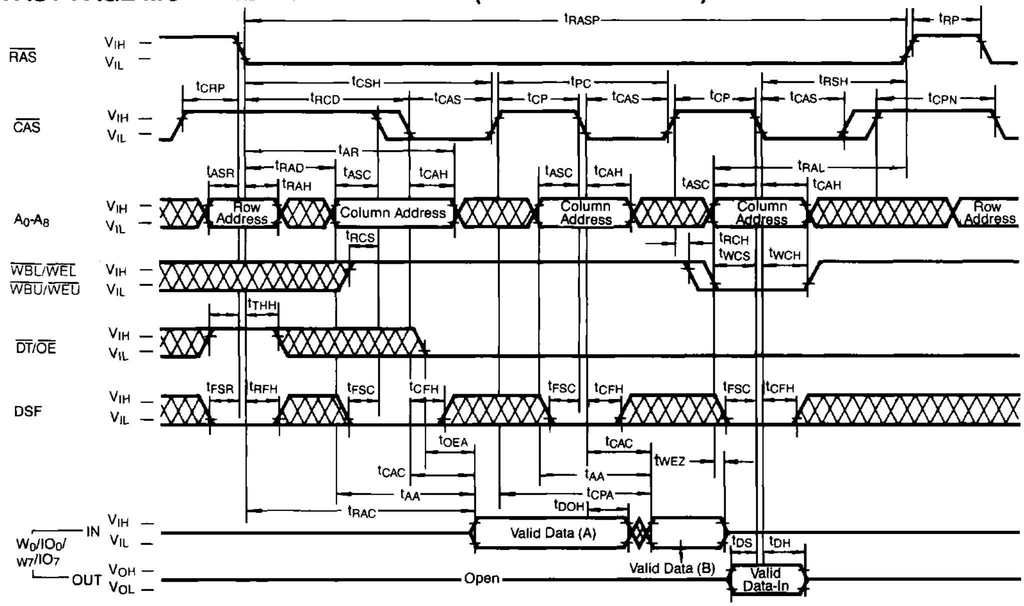
TIMING DIAGRAMS (Continued)

READ-WRITE/READ-MODIFY-WRITE CYCLE

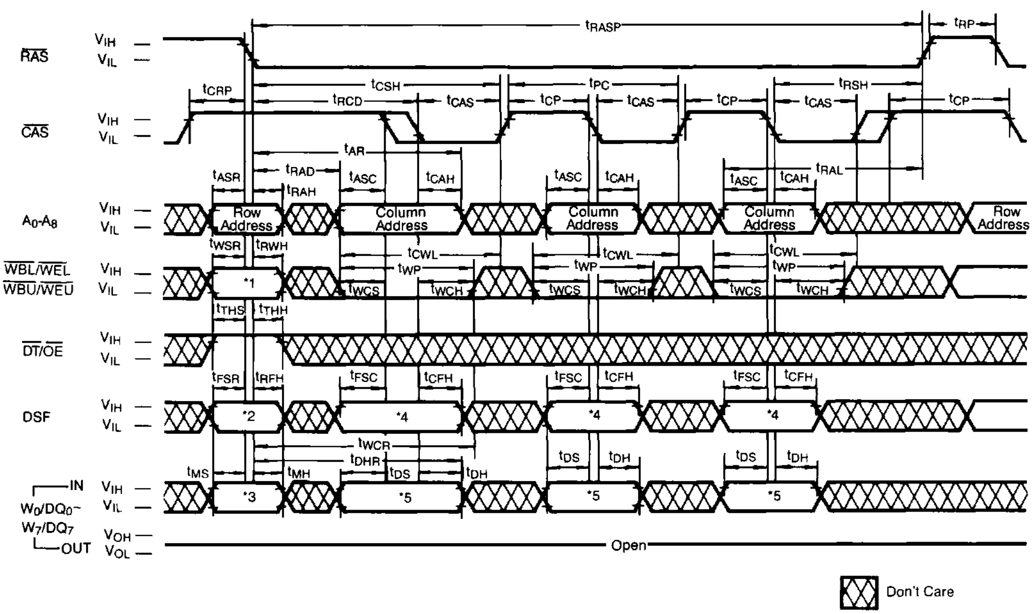


TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ/WRITE CYCLE (Extended Data Out)

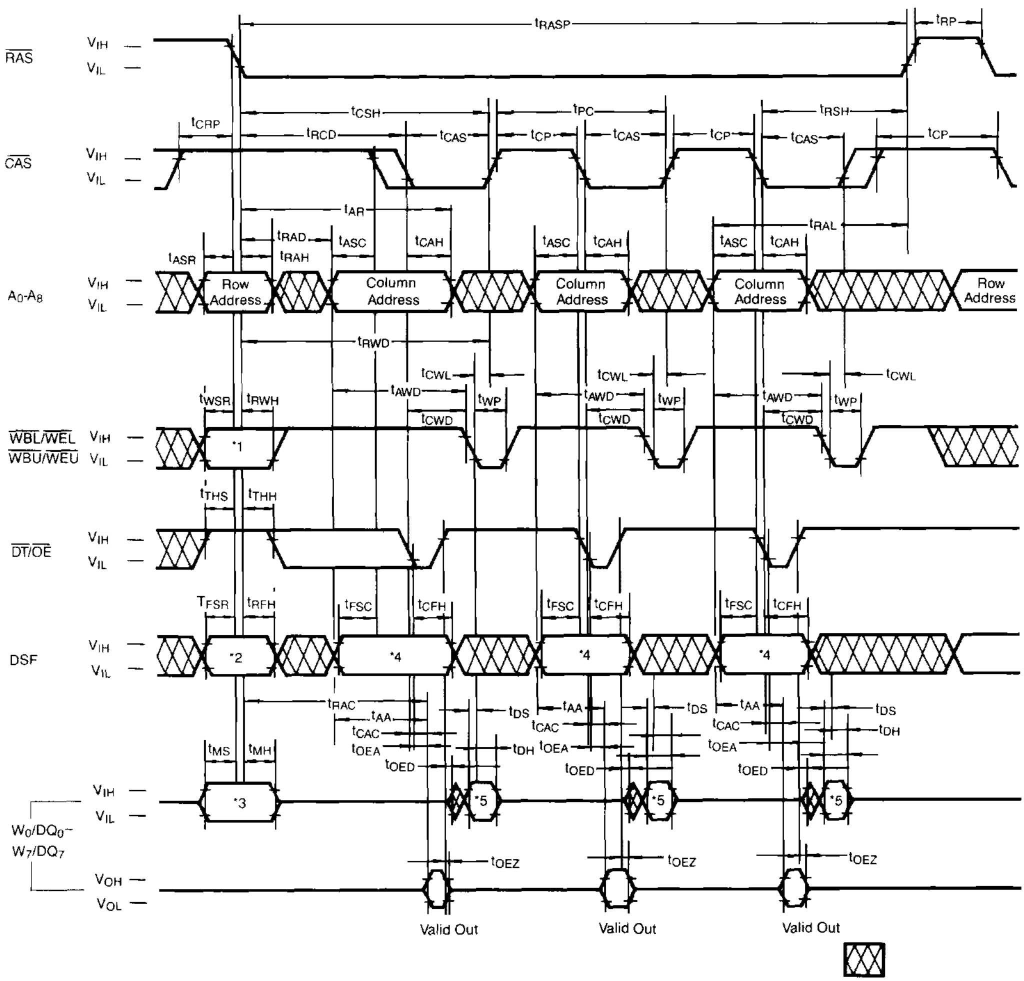


FAST PAGE MODE EARLY WRITE CYCLE



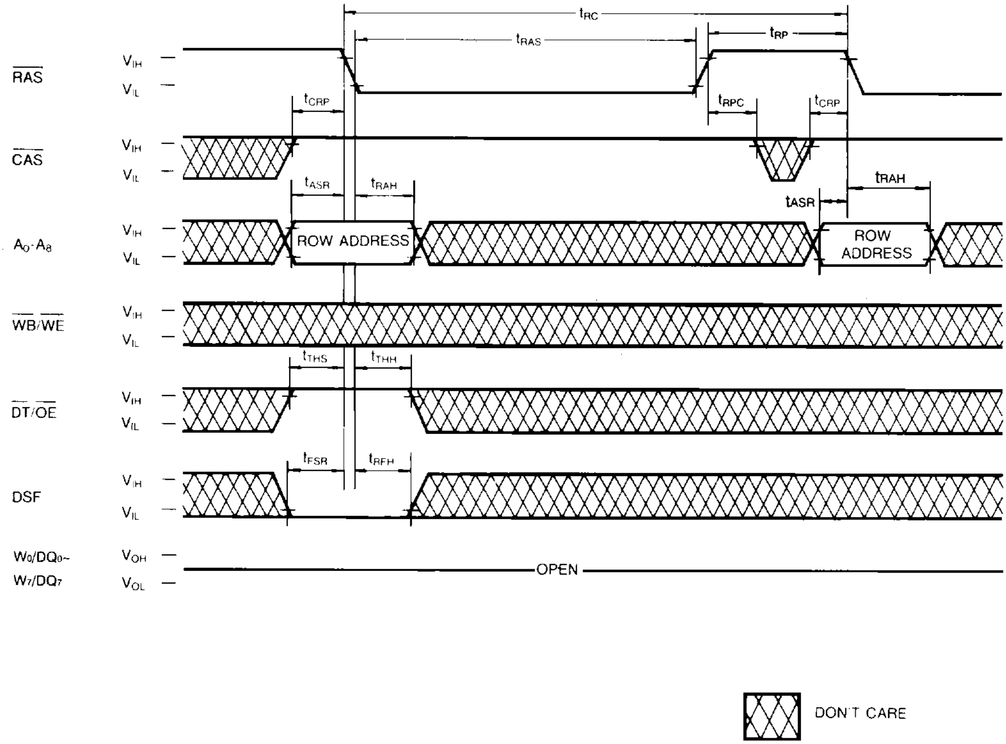
TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ-MODIFY-WRITE CYCLE



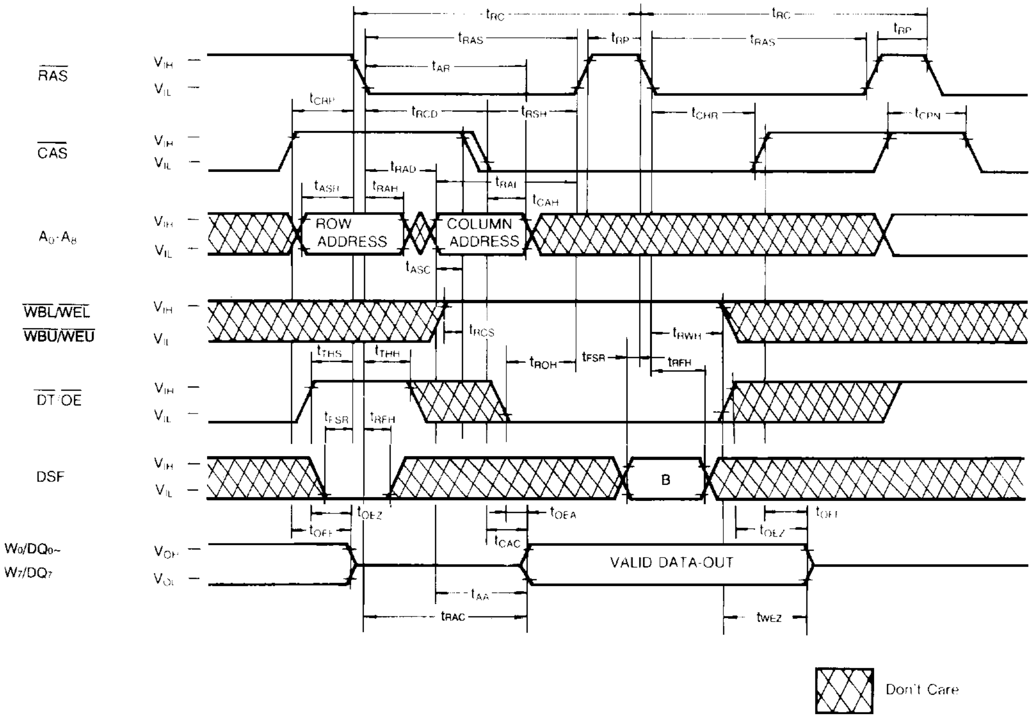
TIMING DIAGRAMS (Continued)

$\overline{RAS}$ ONLY REFRESH CYCLE



TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE



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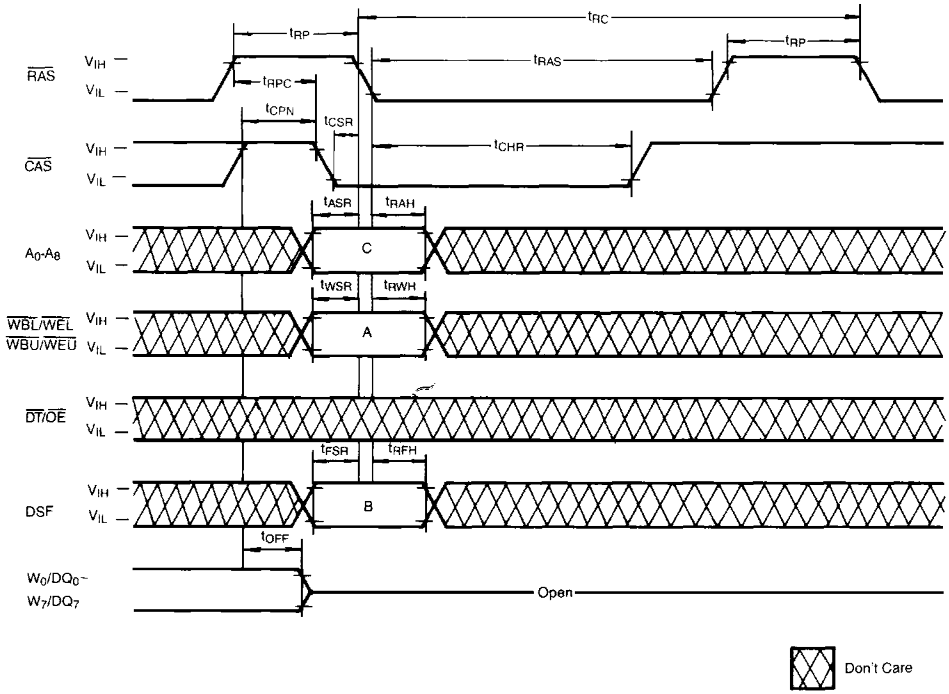
HIDDEN REFRESH CYCLE FUNCTION TABLE

FUNCTION	Logic Status B
Hidden Refresh(Reset All Options)	0
Hidden Refresh(No Reset)	1

TIMING DIAGRAMS (Continued)

CAS BEFORE RAS REFRESH CYCLE

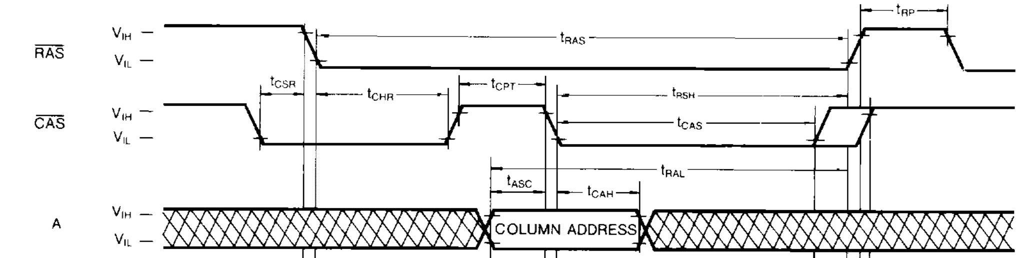


CAS-BEFORE-RAS REFRESH CYCLE FUNCTION TABLE

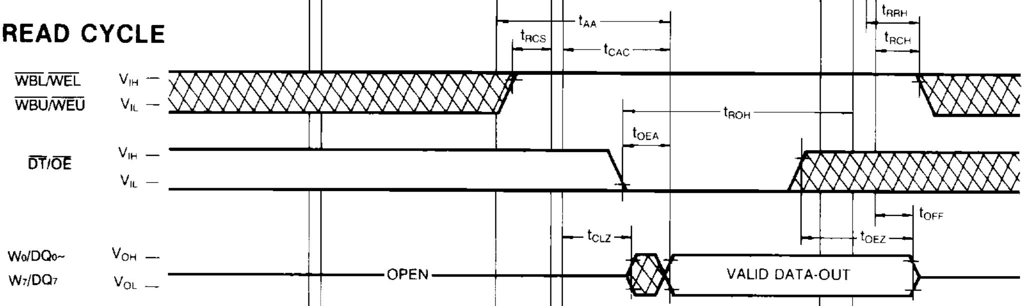
FUNCTION	CODE	LOGIC STATES		
		A	B	C
CAS-BEFORE-RAS REFRESH CYCLE (Reset All Options)	CBRR	X	0	X
CAS-BEFORE-RAS REFRESH CYCLE (Stop Register Set)	CBRS	0	1	Stop Address
CAS-BEFORE-RAS REFRESH CYCLE (No Reset)	CBRN	1	1	X

TIMING DIAGRAMS (Continued)

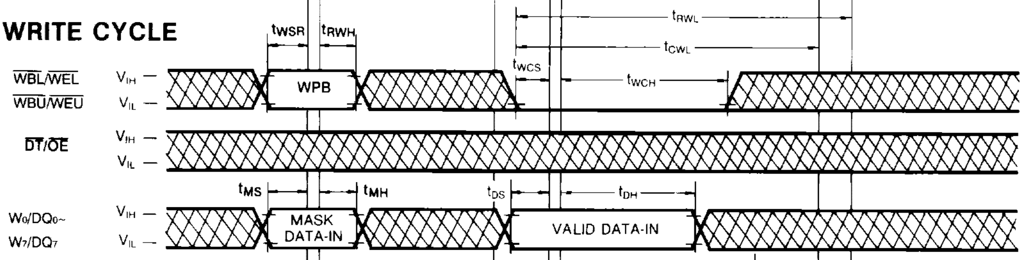
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



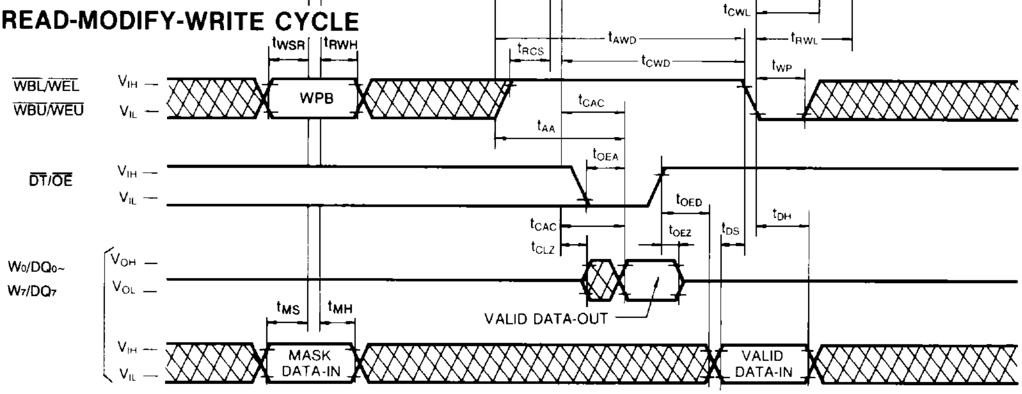
READ CYCLE



WRITE CYCLE



READ-MODIFY-WRITE CYCLE

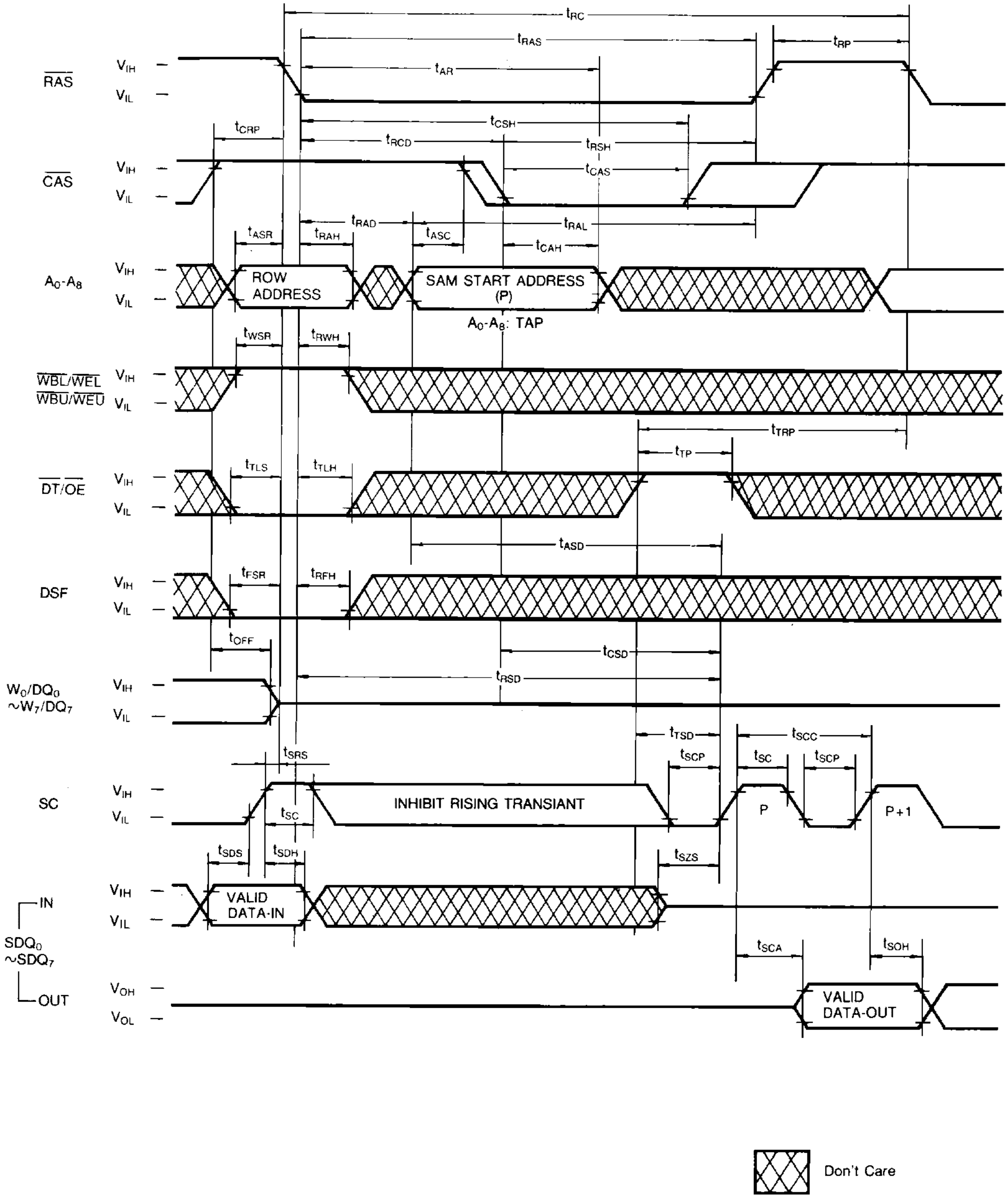


DSF = DON'T CARE

[cross-hatched box] DON'T CARE

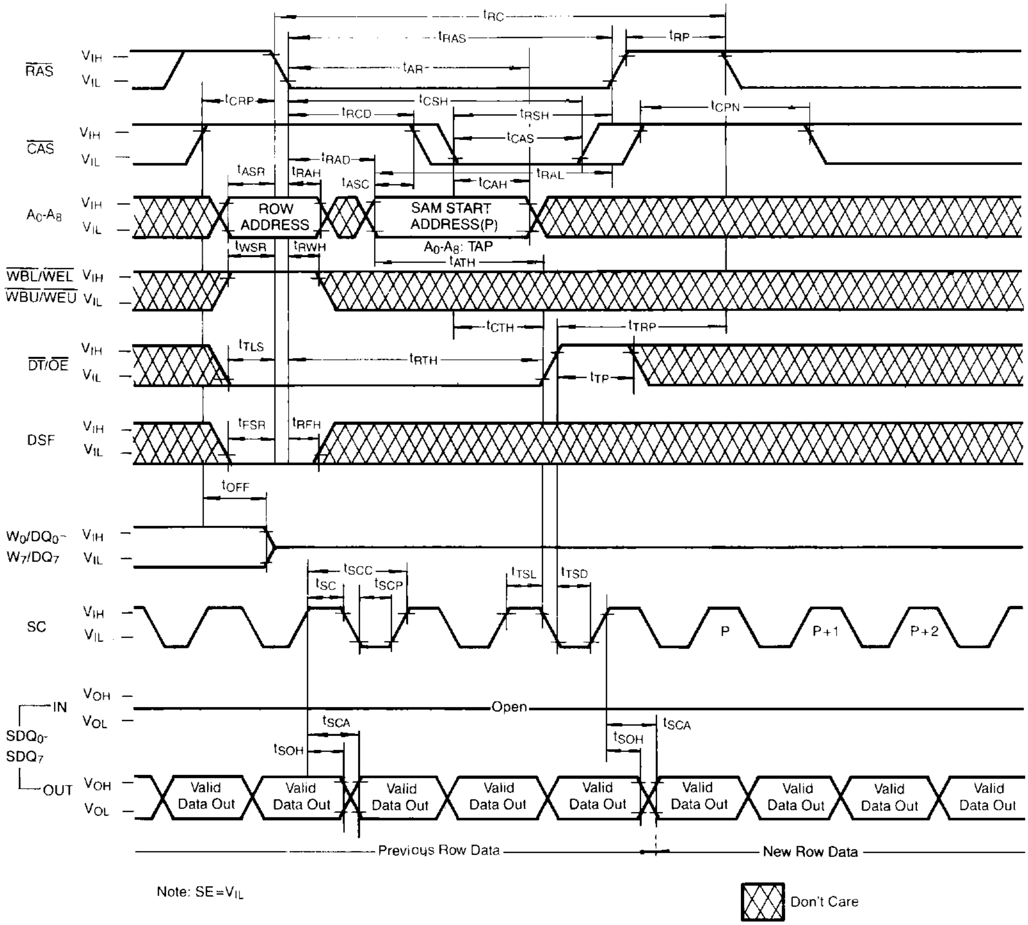
TIMING DIAGRAMS (Continued)

READ TRANSFER CYCLE



TIMING DIAGRAMS (Continued)

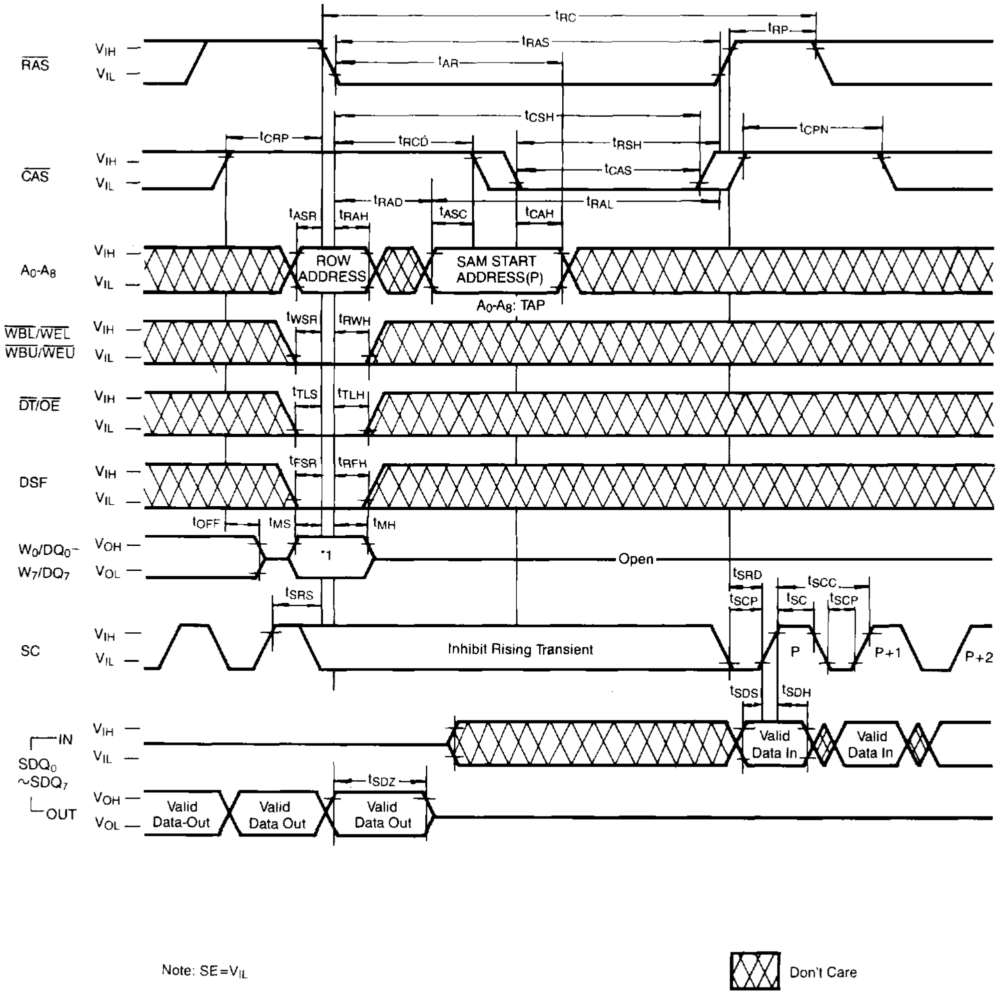
REAL TIME READ TRANSFER CYCLE



2

TIMING DIAGRAMS (Continued)

MASKED WRITE TRANSFER CYCLE (Output Mode to Input Mode Switch)

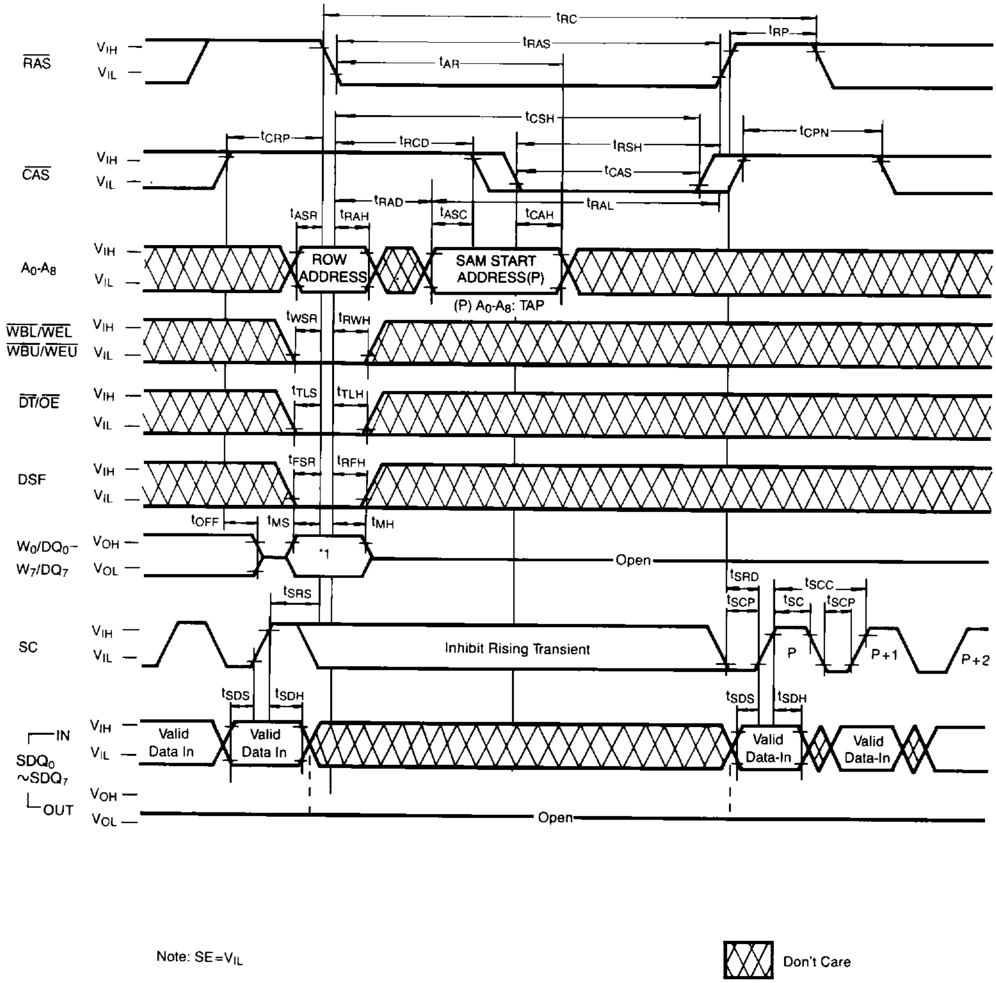


Mask Mode	*1
New Mask Mode	WMi Data
Old Mask Mode	Don't care

WMi Data O: Transfer Disable
1: Transfer Enable

TIMING DIAGRAMS (Continued)

MASKED WRITE TRANSFER CYCLE

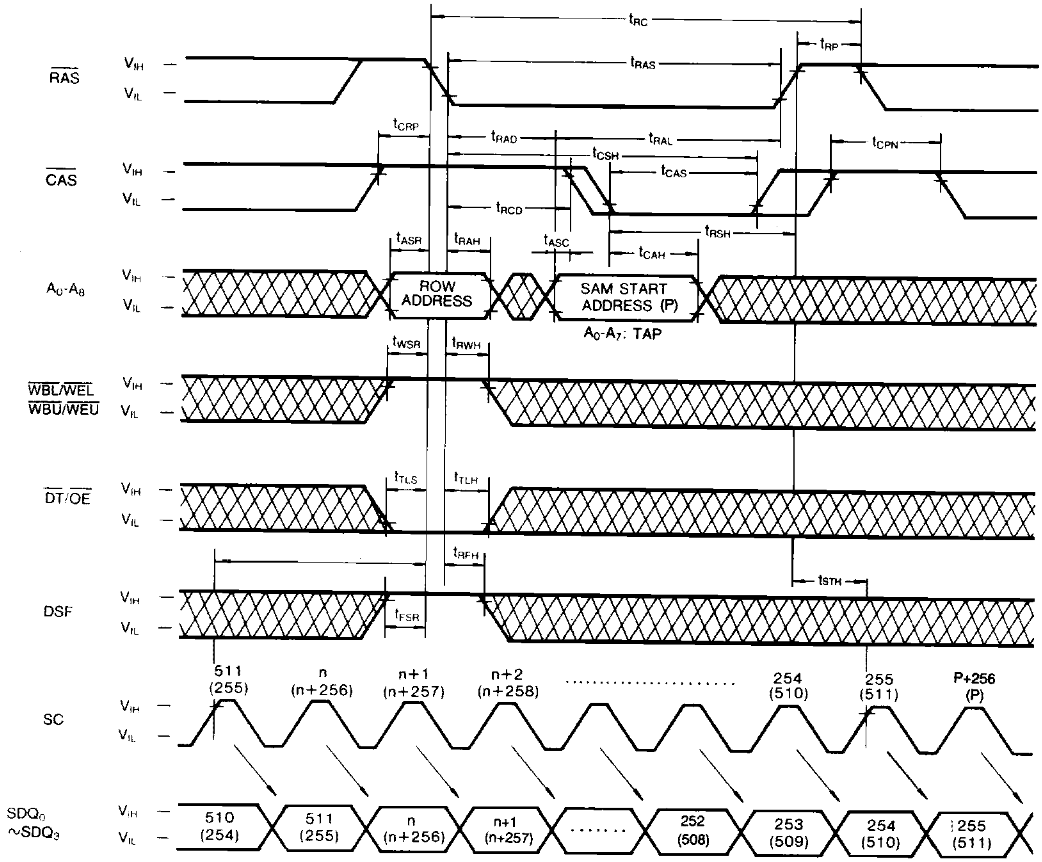


Mask Mode	*1
New Mask Mode	WMi Data
Old Mask Mode	Don't care

WMi Data O: Transfer Disable
1: Transfer Enable

TIMING DIAGRAMS (Continued)

SPLIT READ TRANSFER CYCLE



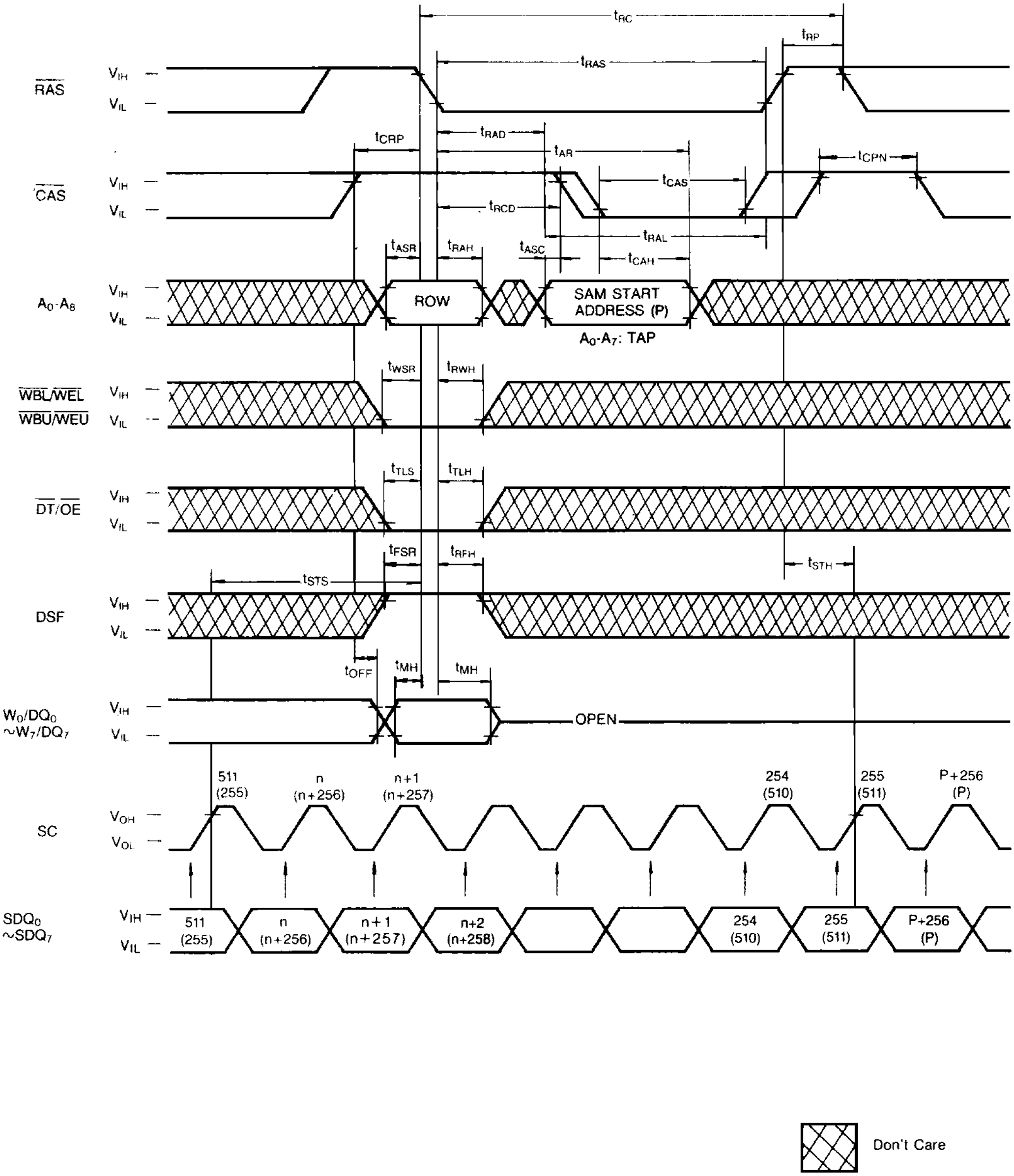
Note: $\overline{SE}=V_{IL}$

Dont' Care

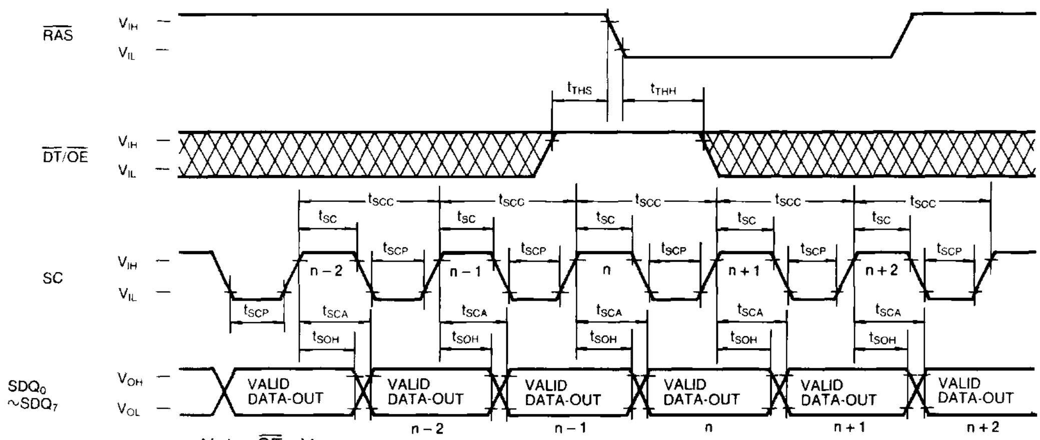
2

TIMING DIAGRAMS (Continued)

MASKED SPLIT WRITE TRANSFER CYCLE

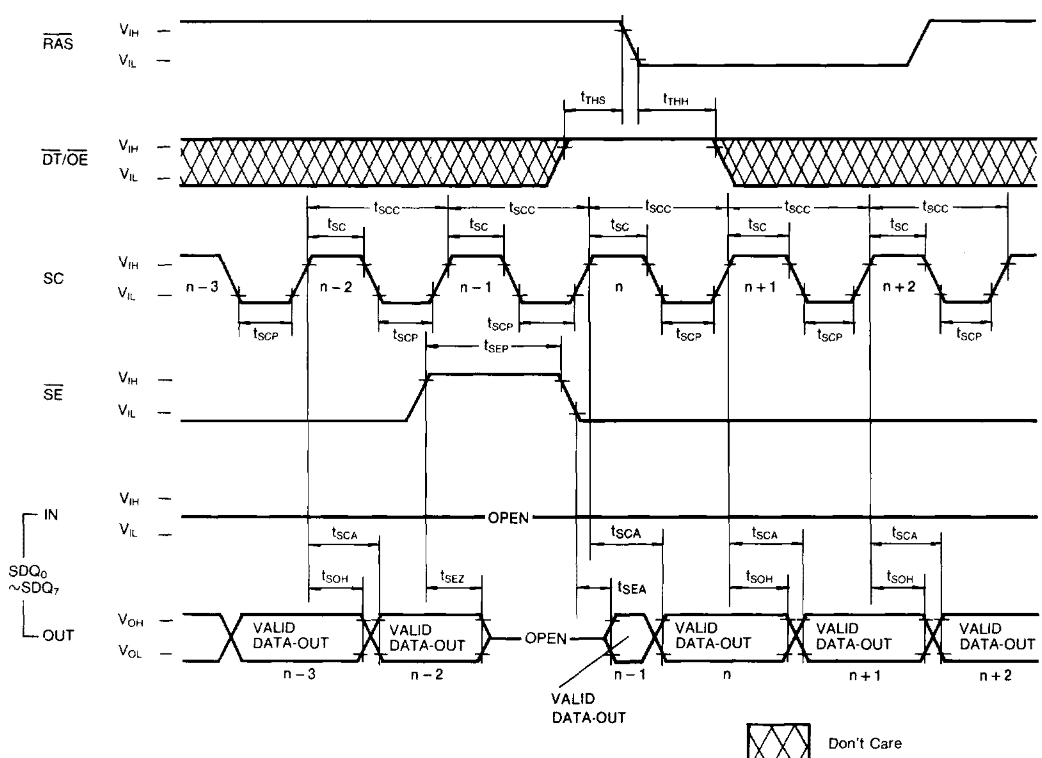


SERIAL READ CYCLE ($\overline{SE} = V_{IL}$)



Note: $\overline{SE} = V_{IL}$

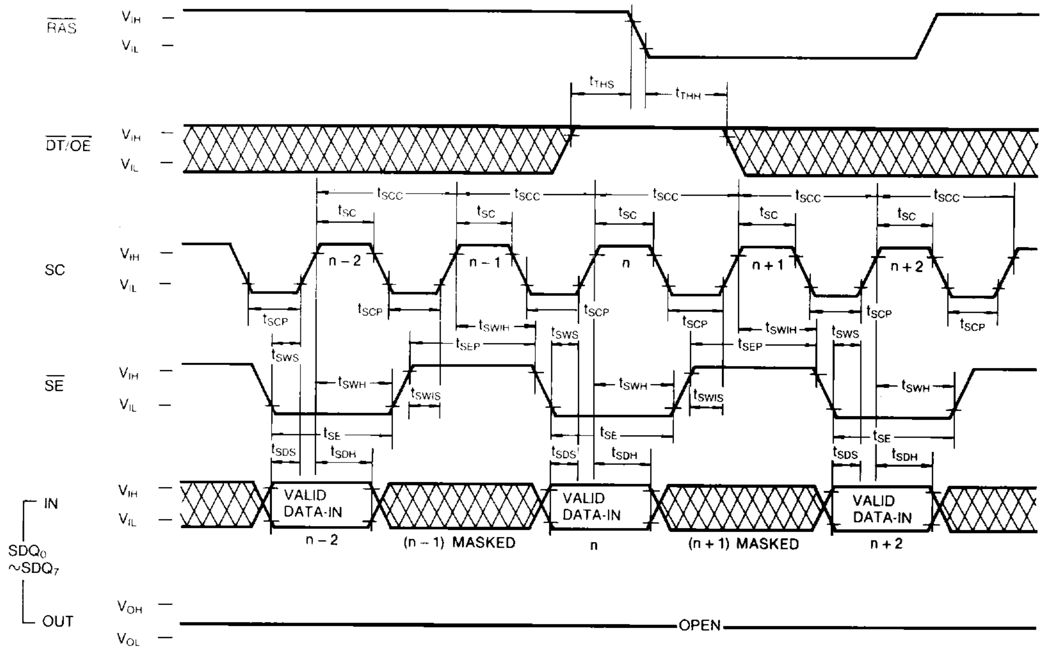
SERIAL READ CYCLE ($\overline{SE}$ Controlled Outputs)



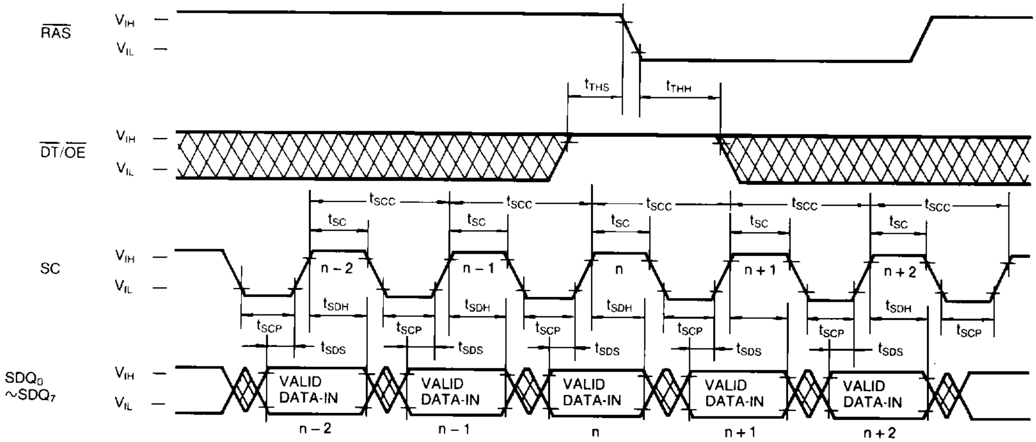
2

TIMING DIAGRAMS (Continued)

SERIAL WRITE CYCLE ($\overline{SE}$ Controlled Inputs)



SERIAL WRITE CYCLE ($\overline{SE} = V_{IL}$)



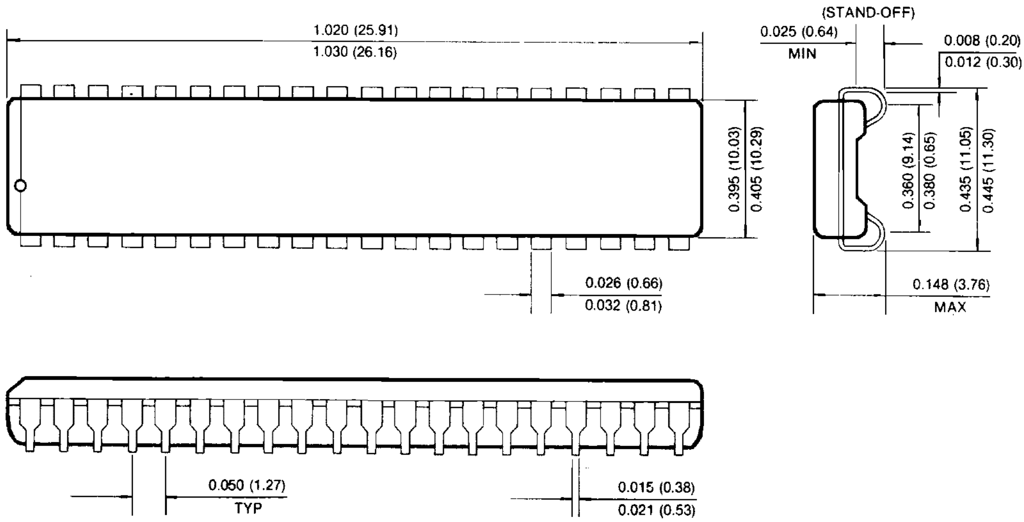
Note: $\overline{SE} = V_{IL}$

Don't Care

PACKAGE DIMENSIONS

40-PIN PLASTIC SOJ

Units: Inches (millimeters)



40/44-PIN PLASTIC TSOP-II (Forward Type)